
Design Example Report

Title	<i>240 W LLC CV/CC Power Supply Using HiperLCS™ LCS708HG and LinkSwitch™-TN LNK302D</i>
Specification	180 VAC – 264 VAC Input; 240 W (48 V at 5 A) Output
Application	Battery Charger
Author	Applications Engineering Department
Document Number	DER-850
Date	January 23, 2020
Revision	3.0

Summary and Features

- Integrated LLC stage for a very low component count design
- 180-264 VAC input (no PFC)
- 120 kHz LLC for wide input/output operating range
- >93% full load efficiency

PATENT INFORMATION

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Important Notes:

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. All testing should be performed using an isolation transformer or isolated sine wave source to provide the AC input to the prototype board.



1 Introduction

This engineering report describes a 48 V (nominal), 240 W reference design operating from 180 VAC to 264 VAC. The power supply is designed with a constant voltage / constant current output for use in battery charger applications. The supply is designed to charge a battery array of 3 parallel strings of X 10 pieces of Sanyo/Panasonic UR18650RX or equivalent cells in series, with a nominal voltage of 42V and a minimum voltage of 24V. The 48V rating of the supply supplies additional headroom.

The design is based on the LCS708HG operating directly from rectified mains, with no PFC input stage. A LNK302DG is utilized in a flyback standby/bias supply. This design poses special challenges in that the primary and secondary voltages of the LLC converter both vary over a wide range.

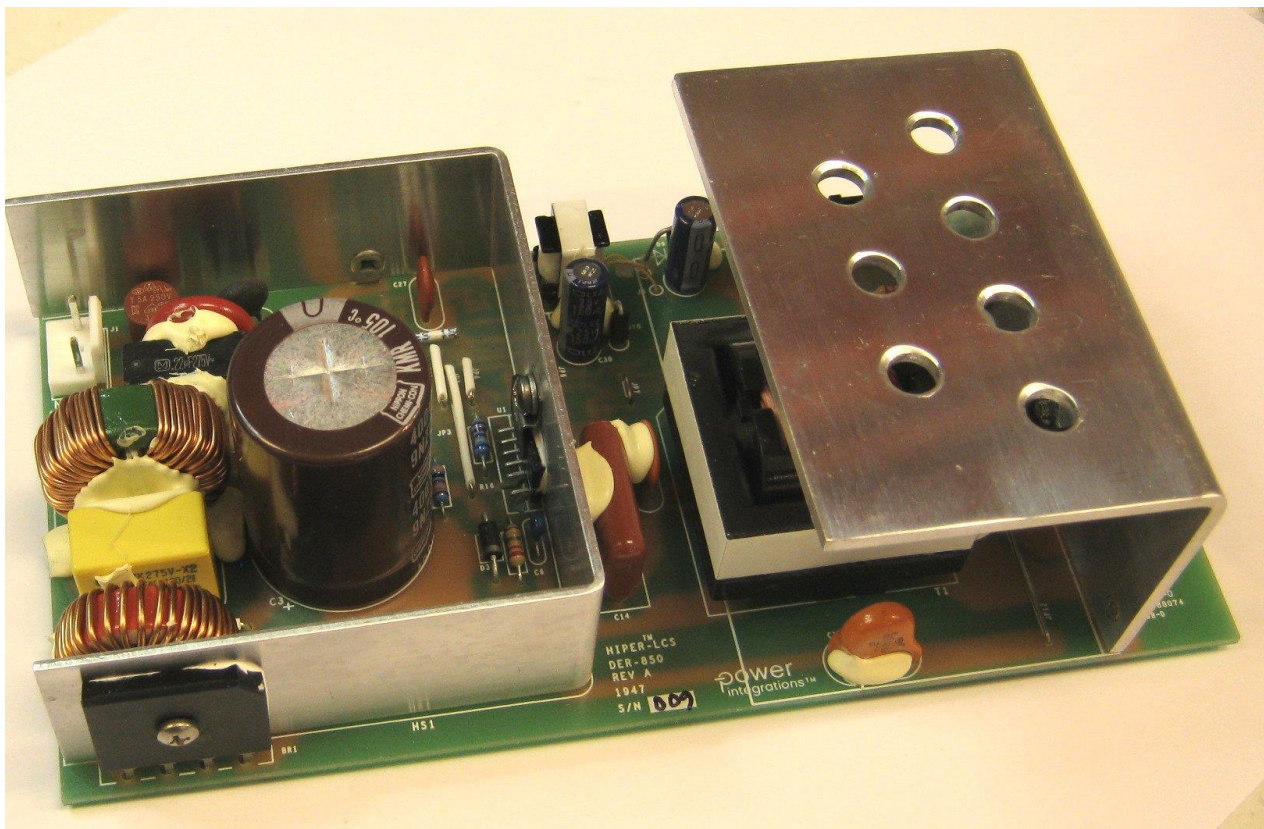


Figure 1 – Photograph, Top View.

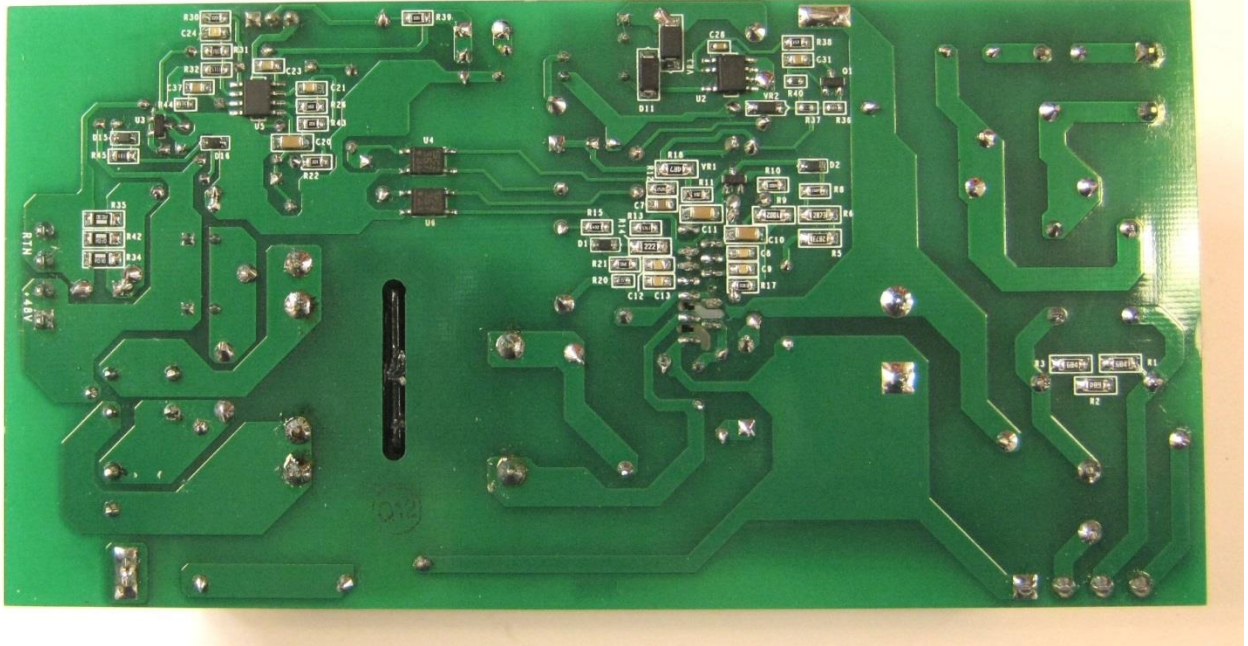


Figure 2 – Photograph, Bottom View.

2 Power Supply Specification

The table below represents the specification for the design detailed in this report. Actual performance is listed in the results section. Detailed customer specification is shown below.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	180		264	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	64	Hz	
Main Converter Output						
Output Voltage	V_{OUT}	0		48	V	48 VDC (Nominal – Otherwise Defined by Battery Load). Nominal Current Limit Setting for Design.
Output Current	I_{OUT}	0		5	A	
Total Output Power						
Continuous Output Power	P_{OUT}		240		W	23 V / 8 A
Peak Output Power	$P_{OUT(PK)}$			N/A	W	
Efficiency						
Total system at Full Load	η_{Main}		93		%	Measured at 230 VAC, Full Load.
Environmental						
Conducted EMI						Meets CISPR22B / EN55022B
Safety						Designed to meet IEC950 / UL1950 Class II
Surge						1.2/50 μ s surge, IEC 1000-4-5, Differential Mode: 2 Ω Common Mode: 12 Ω
Differential					kV	
Common Mode					kV	
Ambient Temperature	T_{AMB}	0		60	$^{\circ}$ C	See Thermal Section for Conditions.

3 Schematic

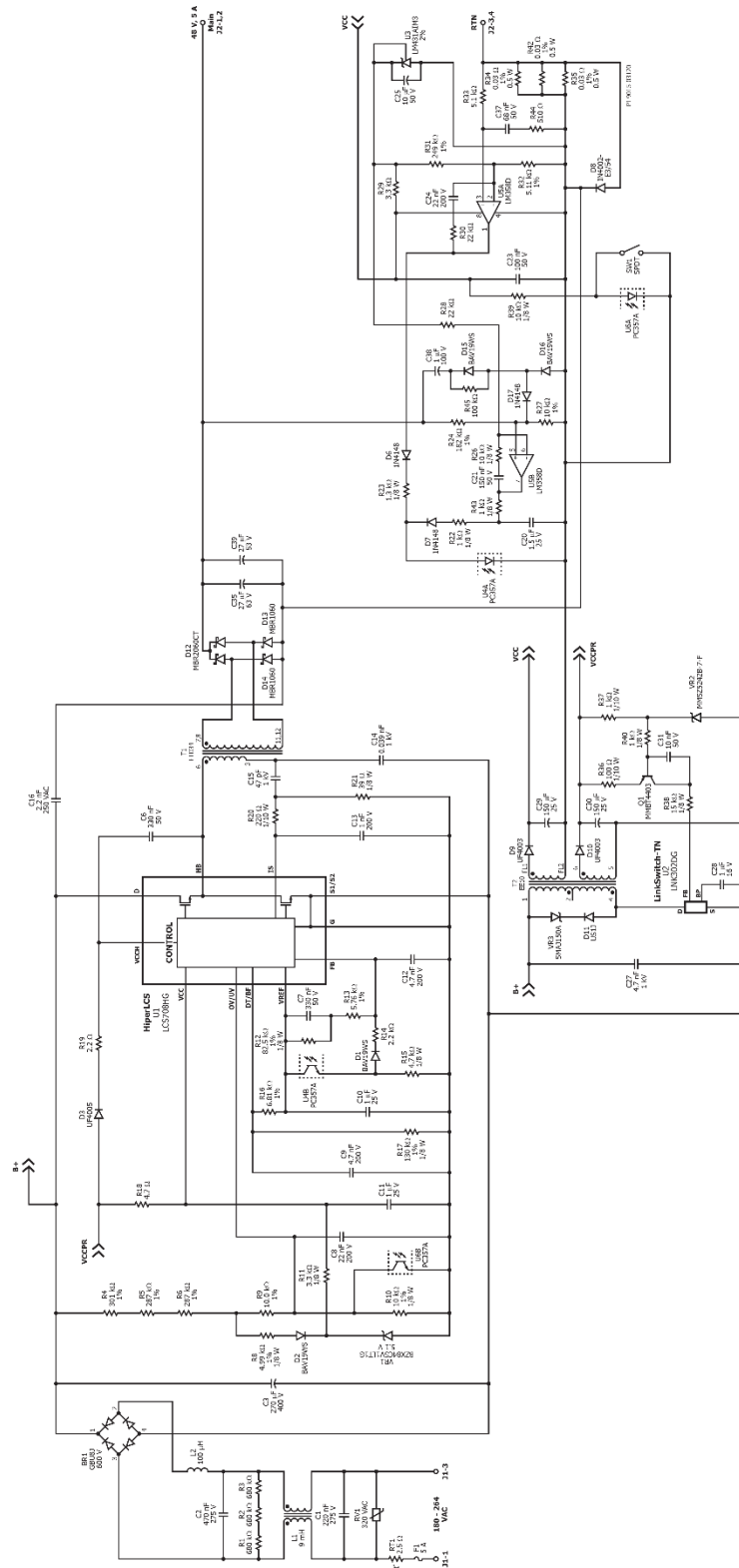


Figure 3 – Schematic, Battery Charger Application Circuit



4 Circuit Description

4.1 General Topology

The schematic in Figure 3 shows an LLC power supply utilizing the LCS708HG, powered by a full wave rectifier from 180 – 264 VAC without a PFC. The LNK302D is used in a flyback bias supply that provides power for both primary and secondary control circuitry. The secondary control circuitry provides CV/CC control for use in battery charger applications

4.2 EMI Filtering / Input Rectifier/Filter

Capacitors C1 and C2 are used to control differential mode noise. Resistors R1-3 discharge C1 and C2 when AC power is removed. Inductor L1 controls common mode EMI. The heat sink for U1 and BR1 is connected to primary return to eliminate the heat sink as a source of radiated/capacitive coupled noise. Thermistor RT1 provides inrush limiting. Capacitor C16 filters common mode EMI. Inductor L2 filters differential mode EMI. Capacitor C3 and BR1 form a full-wave rectifier circuit to provide a ~250-380 VDC B+ supply from the 180-264 VAC input.

4.3 Primary Bias Supply

Components U2, T2, Q1, VR2-3, D11, C27-28, C30-31, R36-38 and R40 comprise a regulated 12 V flyback bias supply for U1. Components D9 and C29 generate a 12 V bias supply for the secondary control circuitry via a triple insulated winding on T2. Zener diode VR3 and D11 protect the U2 drain from leakage spikes.

4.4 LLC Converter

The schematic in Figure 3 depicts a 48 V, 240 W LLC DC-DC converter with constant voltage/ constant current output implemented using the LCS708HG.

Integrated circuit U1 incorporates the control circuitry, drivers and output MOSFETs necessary for an LLC resonant half-bridge (HB) converter. The HB output of U1 drives output transformer T1 via a blocking/resonating capacitor (C14). This capacitor was rated for the operating ripple current and to withstand the high voltages present during fault conditions.

Transformer T1 was designed for a leakage inductance of ~40 μ H. This, along with resonating capacitor C14, sets the primary series resonant frequency at ~127 kHz according to the equation:

$$f_R = \frac{1}{6.28 \sqrt{L_L \times C_R}}$$

Where f_R is the series resonant frequency in Hertz, L_L is the transformer leakage inductance in Henries, and C_R is the value of the resonating capacitor (C14) in Farads.

An operating frequency of ~ 120 kHz was found to be a good compromise between transformer size and operating frequency dynamic range, in view of the wide variation of input and output voltage encountered in this application.

The number of secondary winding turns was chosen to provide a compromise between core and copper losses. AWG #42 Litz wire was used for the primary and AWG #38 for the secondary windings.

The core material selected was Ferroxcube 3F3. This material provided good (low loss) performance.

Components D3, R19, and C6 comprise the bootstrap circuit to supply the internal high-side driver of U1.

Components R18 and C10 provide filtering and bypassing of the +12 V input and the V_{CC} supply for U1. *Note: V_{CC} voltage of >15 V may damage U3.*

Voltage divider resistors R4-10 set the high-voltage brown-in, brown-out, and overvoltage thresholds of U1. The voltage divider values are chosen to set the LLC brown-in at ~ 214 VDC, with an input overvoltage turn-off point (V_{OV}) at 281 VDC. Built-in hysteresis sets the input under voltage brownout point at 189 VDC.

Since a V_{OV} of 281 VDC would cause the power supply to go into overvoltage shutdown before the nominal input voltage of 230 VAC, a "soft clamp" network consisting of components VR1, D2, R8, and R11 is used to change the slope of the input voltage sensing network to allow U1 to operate over a wide range of input voltage without prematurely engaging the U1 OV shutdown. Without this clamp circuit, the supply would start at ~ 150 VAC, but would enter OV shutdown before the nominal 230 VAC operating voltage is reached. A detailed discussion of component selection for proper under and overvoltage points, as well as derivation of the soft clamp network, is shown in section 4.7.

Capacitor C15 forms a current divider with C14, and is used to sample a portion of the primary current. Resistor R21 senses this current, and the resulting signal is filtered by R20 and C13. Capacitor C15 should be rated for the peak voltage present during fault conditions, and should use a stable, low-loss dielectric such as metalized film, SL ceramic, or NPO/COG ceramic. The capacitor used in the DER-850 is a ceramic disc with "COG/NPO" temperature characteristic. The values chosen set the 1 cycle (fast) current limit at 19 A, and the 7-cycle (slow) current limit at 10.6 A, according to the equation:

$$I_{CL} = \frac{0.5}{\left(\frac{C_{15}}{C_{15} + C_{14}} \right) \times R_{21}}$$

I_{CL} is the 7-cycle current limit in Amperes, R_{40} is the current limit resistor in Ohms, and C_{30} and C_{31} are the values of the resonating and current sampling capacitors in nanofarads, respectively. For the one-cycle current limit, substitute 0.9 V for 0.5 V in the above equation. The relatively high setting for the 7-cycle primary current allows sufficient margin for the supply to properly start into a low impedance constant voltage load like a battery.

Resistor R_{20} and capacitor C_{13} filter the primary current signal to the IS pin. Resistor R_{20} is set to 220 Ω , the minimum recommended value. The value of C_{13} is set to 1 nF to avoid nuisance tripping due to noise, but not so large as to substantially affect the current limit set values as calculated above. These components (R_{20} and C_{13}) should be placed close to the IS pin for maximum effectiveness. Because the IS pin can tolerate negative currents, the current sense does not require a complicated rectification scheme.

The Thevenin equivalent combination of R_{16} and R_{17} sets the dead time at 320 ns and maximum operating frequency for U1 at 847 kHz. The DT/BF input of U1 is filtered by C_9 . The combination of R_{16} and R_{17} also selects burst mode "1" for U1. This sets the lower and upper burst threshold frequencies at 382 kHz and 437 kHz, respectively.

The FEEDBACK pin has an approximate characteristic of 2.6 kHz per μA into the FEEDBACK pin. As the current into the FEEDBACK pin increases so does the operating frequency of U1, reducing the output voltage. The series combination of R_{12} and R_{13} sets the minimum operating frequency for U1 at 83 kHz. This value was set to be slightly lower than the frequency required for regulation at full load and minimum bulk capacitor voltage. Resistor R_{12} is bypassed by C_7 to provide output soft start during start-up by initially allowing a higher current to flow into the FEEDBACK pin when the feedback loop is open. This causes the switching frequency to start high and then decrease until the output voltage reaches regulation. Resistor R_{16} is typically set at the same value as the parallel combination of R_{12} and R_{13} so that the initial frequency at soft-start is equal to the maximum switching frequency as set by R_{16} and R_{17} . If the value of R_{16} is less than this, it will cause a delay before switching occurs when the input voltage is applied.

Optocoupler U4 drives the U1 FEEDBACK pin through R_{14} , which limits the maximum optocoupler current into the FEEDBACK pin. Capacitor C_{12} filters the FEEDBACK pin. Resistor R_{15} loads the optocoupler output to force it to run at a relatively high quiescent current, increasing its gain. Resistors R_{14} and R_{15} also improve large signal step response and burst mode output ripple. Diode D1 isolates R_{15} from the F_{MAX} /soft start network.

4.5 **Output Rectification**

The output of transformer T1 is rectified and filtered by D12-14, C35, and C39. Capacitors C35 and C39 are aluminum polymer capacitors chosen for output ripple current rating. Output rectifiers D12-D14 are 60 V Schottky rectifiers chosen for high efficiency. Using a full-wave bridge rectifier instead of a full wave center-tapped configuration eliminates the need to twist transformer secondary winding halves together to improve balancing between phases (improving transformer manufacturability), at the cost of extra power loss in the output rectifier.

4.6 **Output Current and Voltage Control**

Output current is sensed via resistors R34 - R35 and R42. These resistors are clamped by diode D8 to avoid damage to the current control circuitry during an output short circuit. Components R29 and U3 provide a voltage reference for current sense and voltage sense amplifiers U5A and U5B. The reference voltage for current sense amplifier U5A is divided down by R31-32, and filtered by C26. Voltage from the current sense resistors is applied to the non-inverting input of U5A via R33. Opamp U5A drives optocoupler U4 via D6 and R23. Components R23, R30, R33, R44, C24, and C37 are used for frequency compensation of the current loop. Opamp U5B is used for output constant voltage control when the current limit is not engaged. Resistors R24 and R27 sense the output voltage. A reference voltage is applied to the inverting input of U5B from U3 via R28. Opamp U5B drives optocoupler U4 via D7, R22, and R43. Components R22, R26, R28, R43, C20, and C21 all affect the frequency compensation of the voltage control loop.

Components C38, R45, and D15-D17 comprise a soft – finish network to limit the output voltage rate of rise at startup, reducing the amount of output current overshoot when starting into a CV load such as a battery.

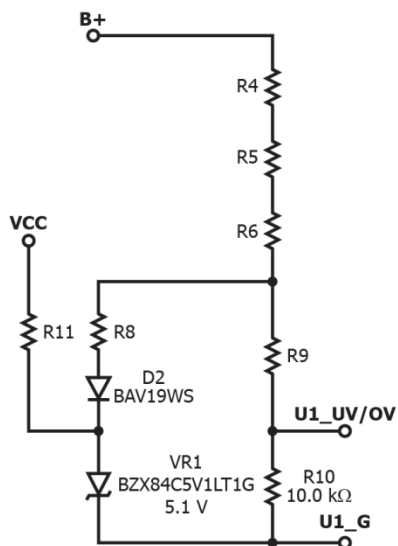
Components R39, SW1, and U6 provide remote start. When SW1 is opened, the output transistor of U6 pulls down on the OV/UV pin of U1, activating undervoltage shutdown. Closing SW1 turns off U6, allowing a normal start-up sequence for U1.

4.7 **Designing Input Undervoltage / Overvoltage Network for U1**

The UV/OV threshold voltages for the HiperLCS are set to a fixed ratio of 131% (nominal), optimized for operation with a boost PFC front end. If this part is used with a standard full-wave rectifier (high line operation) or voltage doubler (low line operation), the B+ voltage range is too wide to be accommodated by using a simple voltage divider to feed the OV/UV pin. If the voltage divider is set so that the HiperLCS starts properly at the low end of the operating range (<180 VAC), the HiperLCS B+ OV protection will cause the device to shut down before the nominal operating voltage of 230 VAC is reached.

There are two solutions to this problem – the first is to clamp the voltage at the UV/OV pin of the HiperLCS so as to disable the OV function. A more desirable solution is to use a

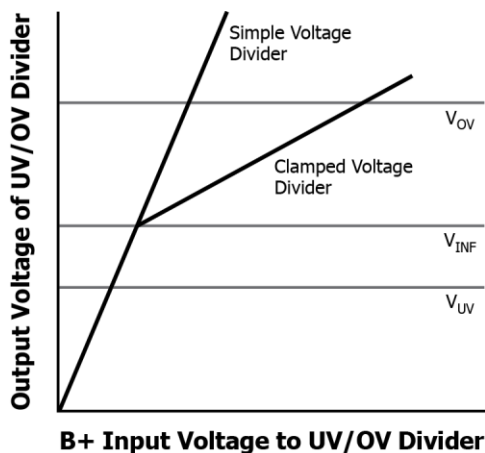
“soft clamp” to shape the output of the UV/OV voltage divider so that OV protection is reached at a higher B+ voltage while still retaining the original UV set point. A circuit to accomplish this is shown in Figure 4.



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Figure 4 – UV/OV Divider Network.

Components R8, R9, R11, D2, and VR1 are used to shape the output voltage characteristics of the divider network as shown in Figure 5, introducing a change of slope that shifts the OV shutdown threshold to a higher B+ voltage.



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Figure 5 – Comparison of Clamped vs. Unclamped UV/OV Voltage Divider Network.

In Figure 5, a clamped voltage divider is compared to a simple unclamped version, showing the curve shaping that allows a higher B+ V_{OV} setting than an unclamped divider while keeping the same V_{UV} set point.

4.7.1 ***Establishing Voltage Set Points***

In order to properly calculate the values needed for the clamped voltage divider network, five voltage set points are needed. These are: the internal V_{UV} and V_{OV} threshold voltages for the HiperLCS IC, the desired B+ low voltage turn-on and OV shutdown thresholds (V_{ON} and V_{OFF}), and the inflection voltage (V_{INF}) where the voltage divider curve changes slope.

4.7.1.1 V_{UV} and V_{OV}

Voltages V_{UV} and V_{OV} are preset inside the HiperLCS IC. The nominal V_{UV} threshold is set at 2.4 V. The nominal V_{OV} threshold is 131% of this value, or 3.14 V. This is covered in the HiperLCS data sheet.

4.7.1.2 V_{ON} and V_{OFF}

In this design example, the operating input voltage range is defined as 180-264 VAC. Since the AC input is feeding a full-wave rectifier, the B+ voltage will be $1.4 \times V_{IN}$, so the nominal B+ will vary from 252-370 VDC. For this exercise, the V_{OFF} point will be set at 400 VDC, sufficiently out of the way of normal operating range to prevent nuisance tripping, but low enough to protect against input voltage swells and surges.

The $V_{BROWNIN}$ voltage is determined by experiment to result in a $V_{BROWNOUT}$ voltage that allows the power supply to start up at low line (180 VAC) when powering up into a voltage source load like a battery. The combined conditions of low line and a voltage source load can prevent the supply from starting. This occurs because the output current overshoots the set value when starting into a voltage source load, due to the finite response time of the CVCC current sense amplifier and the low impedance of the CV output load. This current surge can drag the B+ supply below the brownout threshold at low line, causing the supply to shut down and “hiccup” in a manner similar to an auto-restart event generated by primary overcurrent protection. It is important to place a resistance in series with the electronic load to emulate the characteristic impedance of the battery to be charged, as many electronic loads have impedance on the order of 1 m Ω in CV mode, greatly exacerbating current overshoot. Using the proper impedance in series with the electronic load limits the startup current overshoot to realistic values. In the case of the battery array specified in the introduction of this report, the impedance is ~ 80 m Ω (25 m Ω per cell, 3 parallel strings of 10 cells each). Accordingly, three paralleled 0.24 Ω , 2W resistors were placed in series with the load to approximate the battery impedance.

It is important to remember to adjust the transformer parameters in the design spreadsheet from the initially obtained values so that the power supply will shut down due to $V_{BROWNOUT}$ before gain reversal.

To choose the V_{ON} or $V_{BROWNIN}$ point, PIXIs was used. A V_{BULK_NOM} of 230 VDC was chosen in the PIXIs input parameters – this yields a $V_{ON}/V_{BROWNIN}$ of 214 VDC, as shown in Figure 6, and yields a value of $V_{BROWNOUT}$ that allow the supply to start up into a CV load (with 80 mΩ series impedance) at 180 VAC. The warning for CBULK value shown in Figure 6 should be ignored, as the spreadsheet assumes that the supply is delivering the full power (47 V, 5 A) at brown-in, when in fact the output voltage will be clamped to 42 V or lower.

1	HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
2	▼Enter Input Parameters					Design Title
3	Vbulk_nom	230		230 V		Nominal LLC input voltage
4	Vbrownout			169 V		Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
5	Vbrownin			214 V		Startup threshold on bulk capacitor
6	VOV_shut			281 V		OV protection on bulk voltage
7	VOV_restart			271 V		Restart voltage after OV protection.
8	CBULK	270.00	Warning	270 uF		!!! Warning. CBULK is too small. Recommended value should be greater than 0.7 uF/W
9	tHOLDUP			13.2 ms		Bulk capacitor hold up time
10						

Figure 6 – Using PIXIs to Determine $V_{ON}/V_{BROWNIN}$.

4.7.1.3 Inflection Voltage (V_{INF})

The HiperLCS PIXIs spreadsheet assumes that a normal unclamped voltage divider is used to feed the HiperLCS UV/OV pin. A $V_{BROWNIN}/V_{ON}$ voltage of 214 V, allowing the HiperLCS to turn on and run reliably at 180 VAC, will result in a overvoltage shutdown point (V_{OV_SHUT}) of 281 VDC, as shown on line 6 of Figure 6. For a nominal 230 VAC operating voltage, the B+ is already at $230 \times 1.4 = 322$ VDC, so the OV shutdown feature of the HiperLCS would cause the supply to shut down even before a normal AC operating voltage is reached. This is the reason for using a clamped voltage divider to push up the B+ voltage value where OV shutdown occurs.

To design a clamped voltage divider a voltage V_{INF} (short for $V_{INFLECTION}$) is defined, which sets the B+ voltage at which the V_{OUT} vs. V_{IN} curve of the UV/OV voltage divider changes slope. This should happen somewhat above the nominal low line operating B+ of 230 VDC shown in Figure 6, but comfortably below the unclamped V_{OV_SHUT} of 281 VDC as defined in Figure 6. **For this design example, a V_{INF} of 250 VDC was chosen.**

Table 1 summarizes the voltages necessary for calculating the clamped voltage divider in this design example.

Voltages for Calculating Clamped Voltage Divider				
V_{UV}	V_{OV}	$V_{ON}/V_{BROWNIN}$	V_{OFF}	V_{INF}
2.4 VDC	3.14 VDC	214 VDC	400 VDC	250 VDC

Table 1 – Voltages for Calculating Clamped Voltage Divider Network and Setting Initial Voltage Divider Values.



In order to set the total values for voltage divider string R4-R6, R9, and R10, an initial value for R10 is chosen. In this example, R10 = 10 kΩ was chosen. This yields realizable 1% resistor values for the rest of the resistors in the network. Once R10 is chosen, the top half of the voltage divider (R4 + R5 + R6 + R9 = R_{SUM}) can be calculated using the values for V_{UV} and V_{ON}:

$$R_{SUM} = [R10 (V_{ON}-V_{UV})]/V_{UV} = [10 (214 - 2.4)]/2.4 \approx 882 \text{ k}\Omega$$

This value for R_{SUM} can then be used with the Value for V_{INF} to calculate the value necessary for R9.

V_{INF} is defined as the point at which the slope of the voltage divider changes. This happens when the voltage drop across R9 and R10 is equal to the combined voltage drops of VR1 and D2. VR1 is pre-biased by R11 to its nominal voltage drop of 5.1 V. Diode D2 will barely start conducting at ~0.5 V. Given this, the combined voltage drops add up to 5.6 V, and the value for R9 can be calculated as:

$$R9 = [5.6(R_{SUM} + R10)-(V_{INF} \times R10)]/V_{INF} = [(5.6 \times 892)-2500]/250 = 9.98 \text{ k}\Omega$$

The closest 1% resistor value is 10 kΩ.

Resistor R11 is used to pre-bias Zener diode VR1. This bias current not only applies reverse bias to diode D2 to keep it from conducting prematurely, but also establishes a well-defined voltage drop across VR1. The value chosen for R11 results in a bias current of ~2 mA through VR1.

Since R9 and R_{SUM} are both defined, the rest of the resistors in the R_{SUM} chain can be calculated.

$$R4-R6 = (R_{SUM} - R9)/3 = (882 - 10)/3 = 290.6$$

The closest 1% value is 287 kΩ. Three resistors of this value in series yields 861 kΩ for R_{SUM}, short of the necessary value of 872 kΩ. To adjust the value of R_{SUM} closer to the required value, R4 is changed to 301 kΩ, yielding 875 kΩ for R_{SUM}. These values will be used in subsequent calculations (R4 = 301 kΩ, R5-6 = 287 kΩ).

4.7.1.4 Setting Clamp Resistor R8

In order to set the proper value for clamp resistor R8, it first necessary to find the voltage V_{SD} across R9 and R10 that will result in OV shutdown for U1. This will be the voltage across R9 and R10 that will provide 3.14 V to the U1 UV/OV pin.

$$V_{SD} = V_{OV} [1 + (R9/R10)] = 3.14 (1 + 1) = 6.28 \text{ V}$$

This is the voltage across R9 and R10 necessary to reach the OV threshold at the UV/OV pin of U1.

It is next necessary to calculate voltage V_{SD}' at the junction of R6 and R9 at the B+ shutdown voltage V_{OFF} of 400 VDC. **This voltage is calculated as if R8 is open.**

$$V_{SD}' = 400[(R9 + R10)/(R4 + R5 + R6 + R9 + R10)] = 8.94 \text{ V}$$

Using V_{SD} and V_{SD}' , we can now set up the calculation for R8.

The voltage divider of R4-6, R9, and R10 driven by the V_{OFF} B+ value of 400 V can be re-expressed as a voltage source V_{SD}' driving a Thevenin equivalent resistance. The Thevenin resistance R_{TH} is equivalent to the parallel combination of the top and bottom halves of the voltage divider:

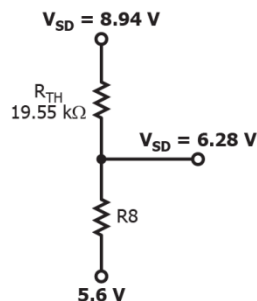
$$R_{TH} = (R4 + R5 + R6) // (R9 + R10) = 875 \text{ k} // 20 \text{ k} = 19.55 \text{ k}\Omega$$

Once this is determined, the voltage divider and clamp can be reduced to the schematic shown in Figure 7.

From the simple equivalent schematic of Figure 7, it is straightforward to calculate R8:

$$R8 = R_{TH} (V_{SD} - 5.6)/(V_{SD}' - V_{SD}) = (19.55(6.28 - 5.6))/(8.94 - 6.28) = 4.99 \text{ k}\Omega$$

The nearest 1% value is 4.99 k Ω



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Figure 7 – Voltage Divider and Clamp Thevenin Equivalent for Calculating R8.

5 PCB Layout

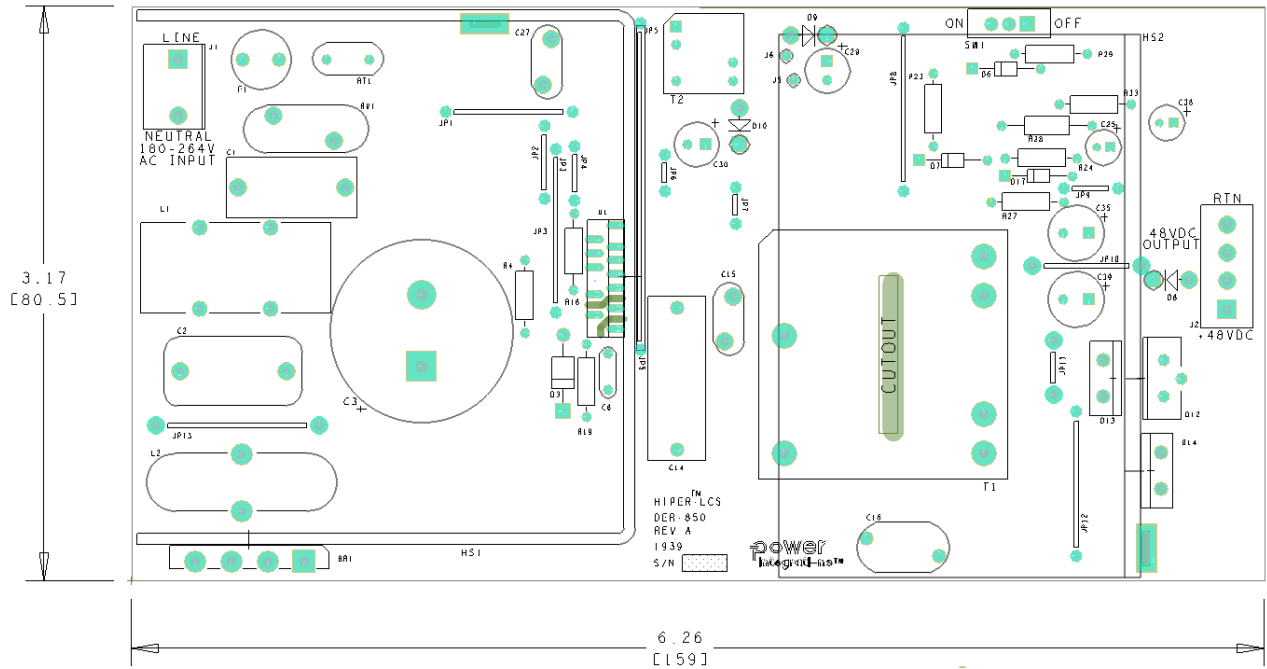


Figure 8 – Printed Circuit Layout, Top Side.

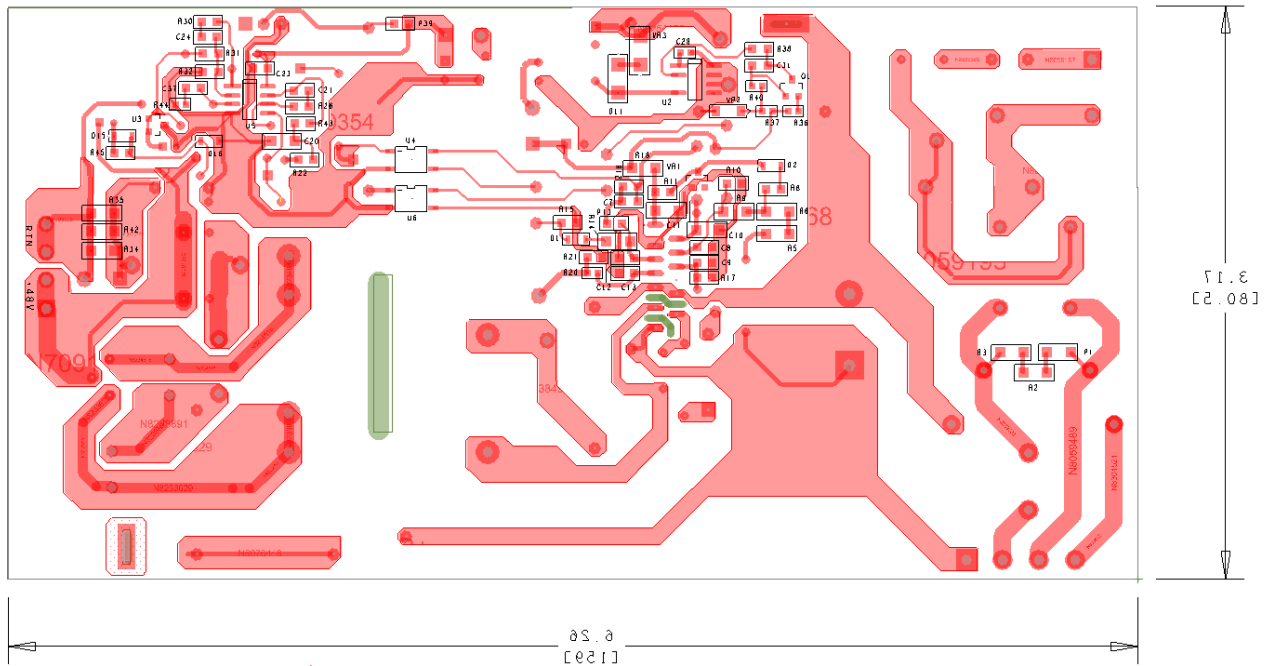


Figure 9 – Printed Circuit Layout, Bottom Side.



6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 8 A, Bridge Rectifier, GBU Case	GBU8J-BP	Micro Commercial
2	1	C1	220 nF, 275 VAC, Film, X2	ECQ-U2A224ML	Panasonic
3	1	C2	470 nF, 275 VAC, Film, X2	PX474K31D5	Carli
4	1	C3	270 μ F, 400 V, Electrolytic, (25.4 x 35)	EKMR401VSN271MQ35S	UCC
5	1	C6	330 nF, 50 V, Ceramic, X7R	FK24X7R1H334K	TDK
6	1	C7	330 nF, 50 V, Ceramic, X7R, 0805	GRM219R71H334KA88	Murata
7	2	C8 C24	22 nF, 200 V, Ceramic, X7R, 0805	08052C223KAT2A	AVX
8	2	C9 C12	4.7 nF, 200 V, Ceramic, X7R, 0805	08052C472KAT2A	AVX
9	2	C10 C11	1 μ F, 25 V, Ceramic, X7R, 1206	C3216X7R1E105K	TDK
10	1	C13	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
11	1	C14	0.039 μ F, \pm 3%, 1000 V, Metal Polypropylene Film, (23.00 mm x 8.00 mm)	ECW-H10393HV	Panasonic
12	1	C15	47 pF, 1000 V, Disc Ceramic	561R10TCCQ47	Vishay
13	1	C16	2.2 nF, Ceramic, Y1	440LD22-R	Vishay
14	1	C20	1.5 μ F, \pm 20%, 25 V, Ceramic, X7R, 1206	CGA5L2X7R1E155M160AA	TDK
15	1	C21	150 nF, 50 V, Ceramic, X7R, 0805	CL21B154KBFNNNE	Samsung
16	1	C23	100 nF, 50 V, Ceramic, X7R, 0805	CC0805KRX7R9BB104	Yageo
17	1	C25	10 μ F, 50 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG500ELL100ME11D	Nippon Chemi-Con
18	1	C27	4.7 nF, 1 kV, Thru Hole, Disc Ceramic	562R5GAD47	Vishay
19	1	C28	1 μ F, 16 V, Ceramic, X5R, 0603	GRM188R61C105KA93D	Murata
20	2	C29 C30	150 μ F, 25 V, Electrolytic, Low ESR, 180 m Ω , (6.3 x 15)	ELXZ250ELL151MF15D	Nippon Chemi-Con
21	1	C31	10 nF, 50 V, Ceramic, X7R, 0805	C0805C103K5RACTU	Kemet
22	2	C35 C39	27 μ F, 20%, 63 V, Aluminum Polymer Electrolytic, Low ESR, 33 m Ω , 3000 Hrs @ 105°C, (8 x 12)	PLV1J270MDL1TD	Nichicon
23	1	C37	68 nF, 50 V, Ceramic, X7R, 0805	C0805C683K5RACTU	Kemet
24	1	C38	1 μ F, 100 V, Electrolytic, Gen. Purpose, (5 x 11)	EKMG101ELL1R0ME11D	Nippon Chemi-Con
25	4	D1 D2 D15 D16	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diode Inc.
26	1	D3	600 V, 1 A, Ultrafast Recovery, 75 ns, DO-41	UF4005-E3	Vishay
27	3	D6 D7 D17	75 V, 300 mA, Fast Switching, DO-35	1N4148TR	Vishay
28	1	D8	100 V, 1 A, Rectifier, DO-41	1N4002-E3/54	Vishay
29	2	D9 D10	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
30	1	D11	DIODE ULTRA FAST, SW 600 V, 1A, SMA	US1J-13-F	Diodes, Inc.
31	1	D12	60 V, 20 A, Dual Schottky, TO-220AB	MBR2060CT	Vishay
32	2	D13 D14	60 V, 10 A, Schottky, TO-220AC	MBR1060	Vishay
33	1	ESIP CLIP1	Heat sink, Edge Clip, 12.40 mm x 6.50 mm	TRK-24	Kang Tang Hardware
34	1	F1	5 A, 250V, Slow, TR5	37215000411	Wickman
35	1	HS1	FAB, Heat sink, BRIDGE_Esip, DER447		Custom
36	1	HS2	FAB, Secondary Heat sink, DER850_PRIMARY		Power Integrations
37	1	J1	3 Position (1 x 3) header, 0.156 pitch, Vertical	B3P-VH	JST
38	1	J2	4 Position (1 x 4) header, 0.156 pitch, Vertical	26-48-1045	Molex
39	1	JP1	Wire Jumper, Insulated, TFE, #22 AWG, 0.7 in	C2004-12-02	Alpha
40	1	JP2	Wire Jumper, Non insulated, #22 AWG, 0.4 in	298	Alpha
41	2	JP3 JP8	Wire Jumper, Insulated, #24 AWG, 0.9 in	C2003A-12-02	Gen Cable
42	1	JP4	Wire Jumper, Insulated, #24 AWG, 0.3 in	C2003A-12-02	Gen Cable
43	1	JP5	Wire Jumper, Insulated, #24 AWG, 1.8 in	C2003A-12-02	Gen Cable
44	2	JP6 JP7	Wire Jumper, Non insulated, #22 AWG, 0.2 in	298	Alpha
45	1	JP9	Wire Jumper, Non insulated, #22 AWG, 0.3 in	298	Alpha
46	1	JP10	Wire Jumper, Insulated, TFE, #18 AWG, 0.6 in	C2052A-12-02	Alpha



47	1	JP11	Wire Jumper, Insulated, TFE, #18 AWG, 0.3 in	C2052A-12-02	Alpha
48	1	JP12	Wire Jumper, Non insulated, #22 AWG, 0.8 in	298	Alpha
49	1	JP13	Wire Jumper, Insulated, TFE, #18 AWG, 0.9 in	C2052A-12-02	Alpha
50	1	L1	9 mH, 5 A, Common Mode Chokey	T22148-902S P.I. Custom	Fontaine Tech
51	1	L2	100 μ H, 5 A, INDUCTOR TORD HI AMP 100 UH VERT	7447070	Würth
52	3	NUT1 NUT2 NUT3	Nut, Hex, Kep 4-40, S ZN Cr3 plating RoHS	4CKNTZR	Any RoHS Compliant Mfg.
53	1	Q1	PNP, Small Signal BJT, 40 V, 0.6 A, SOT-23	MMBT4403-7-F	Diodes, Inc.
54	3	R1 R2 R3	RES, 680 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ684V	Panasonic
55	1	R4	RES, 301 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-301K	Yageo
56	2	R5 R6	RES, 287 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2873V	Panasonic
57	1	R8	RES, 4.99 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF4991V	Panasonic
58	1	R9	RES, 10.0 k Ω , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1002V	Panasonic
59	1	R10	RES, 10.0 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1002V	Panasonic
60	1	R11	RES, 3.3 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ332V	Panasonic
61	1	R12	RES, 82.5 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF8252V	Panasonic
62	1	R13	RES, 5.76 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5761V	Panasonic
63	1	R14	RES, 33 k Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ222V	Panasonic
64	1	R15	RES, 4.7 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ472V	Panasonic
65	1	R16	RES, 6.81 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-6K81	Yageo
66	1	R17	RES, 130 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1303V	Panasonic
67	1	R18	RES, 4.7 Ω , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ4R7V	Panasonic
68	1	R19	RES, 2.2 Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-2R2	Yageo
69	1	R20	RES, 220 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ221V	Panasonic
70	1	R21	RES, 39 Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ390V	Panasonic
71	2	R22 R43	RES, 1 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ102V	Panasonic
72	1	R23	RES, 1.3 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-1K3	Yageo
73	1	R24	RES, 182 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-182K	Yageo
74	2	R26 R39	RES, 10 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ103V	Panasonic
75	1	R27	RES, 10.0 k Ω , 1%, 1/4 W, Metal Film	MFR-25FBF-10K0	Yageo
76	1	R28	RES, 22 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-22K	Yageo
77	1	R29	RES, 3.3 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-3K3	Yageo
78	1	R30	RES, 22 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ223V	Panasonic
79	1	R31	RES, 249 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF2493V	Panasonic
80	1	R32	RES, 5.11 k Ω , 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5111V	Panasonic
81	1	R33	RES, 5.1 k Ω , 5%, 1/4 W, Carbon Film	CFR-25JB-5K1	Yageo
82	3	R34 R35 R42	RES, 0.03 Ω , 1%, 1/4 W, Thick Film, 1206, ± 100 ppm/ $^{\circ}$ C, -55 $^{\circ}$ C ~ 155 $^{\circ}$ C	PF1206FRF070R03L	Yageo
83	1	R36	RES, 100 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
84	2	R37 R40	RES, 1 k Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
85	1	R38	RES, 15 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ153V	Panasonic
86	1	R44	RES, 510 Ω , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ511V	Panasonic
87	1	R45	RES, 100 k Ω , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
88	1	RT1	NTC Thermistor, 2.5 Ω , 5 A	SL10 2R505	Ametherm
89	1	RTV1	Thermally conductive Silicone Grease	120-SA	Wakefield
90	1	RV1	320 VAC, 80 J, 14 mm, RADIAL	V320LA20AP	Littlefuse
91	2	SCREW1 SCREW2	SCREW MACHINE PHIL 4-40 X 5/16 SS	PMSSS 440 0031 PH	Building Fasteners
92	1	SCREW3	SCREW MACHINE PHIL 4-40 X 3/8 SS	PMSSS 440 0038 PH	Building Fasteners
93	1	SCREW4	SCREW MACHINE PHIL 4-40 X 1/2 SS	PMSSS 440 0050 PH	Building Fasteners
94	1	SW1	SWITCH SLIDE SPDT 30V .2A PC MNT	EG1218	E-Switch
95	1	T1	DER-850 LLC Transformer Rev 3	25-01172-00	PI
96	1	T2	DER-850 Bias Transformer Rev 1	25-01168-00	PI
97	3	TO-220 PAD1 TO-	THERMAL PAD TO-220 .009" SP1000	1009-58	Bergquist

		220 PAD2 TO-220 PAD3			
98	1	U1	HiperLCS, ESIP16/13	LCS708HG	Power Integrations
99	1	U2	LinkSwitch-TN, SO-8	LNK302DN	Power Integrations
100	1	U3	IC, REG ZENER SHUNT ADJ SOT-23	LM431AIM3/NOPB	National Semi
101	2	U4 U6	Optoisolator, Transistor Output, 3750 Vrms, 1 Channel, 4-Mini-Flat	PC357N1J000F	Sharp
102	1	U5	DUAL Op Amp, Single Supply, SOIC-8	LM358D	Texas Instruments
103	1	VR1	5.1 V, 5%, 250 mW, SOT23	BZX84C5V1LT1G	On Semi
104	1	VR2	DIODE ZENER 12 V 500 mW SOD123	MMSZ5242B-7-F	Diodes, Inc.
105	1	VR3	150 V, 1 W, 243 V, SMA, DO214AC (SMA)	SMAJ150A-13-F	Diodes, Inc.
106	6	WASHER1 WASHER2 WASHER3 WASHER4 WASHER5 WASHER6	WASHER FLAT #4 Zinc, OD 0.219, ID 0.125, Thk 0.032, Yellow Chromate Finish	5205820-2	Tyco
107	3	WASHER7 WASHER8 WASHER9	Washer ,Shoulder, #4, 0.032 Shoulder x 0.116" Dia, Polyphenylene Sulfide PPS	7721-7PPSG	Aavid Thermalloy

7 Magnetics

7.1 LLC Transformer (T1) Specification

7.1.1 Electrical Diagram

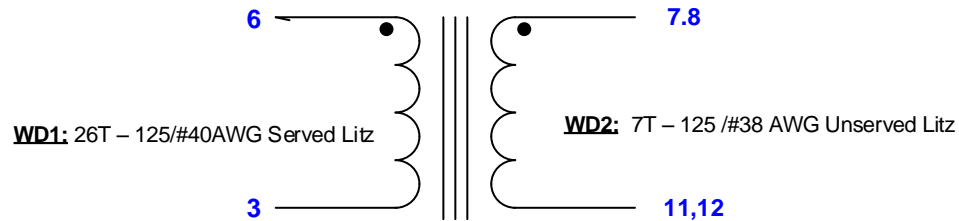


Figure 10 – LLC Transformer Schematic.

7.1.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 3-6 to pins 7-12.	3000 VAC
Primary Inductance	Pins 3-6 all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	160 μH ±10%
Resonant Frequency	Pins 3-6, all other windings open.	2,400 kHz (Min.)
Primary Leakage Inductance	Pins 3-6, with pins 7,8 and 11,12 shorted, measured at 100 kHz, 0.4 V _{RMS} .	40 μH ±5%

7.1.3 Material List

Item	Description
[1]	Core Pair ETD34: Ferroxcube 3F3 or equivalent, gap for A _{L,G} of 237 nH/T ² .
[2]	Bobbin: Winshine WS-53404; PI#: 25-01048-00.
[3]	Bobbin Cover: Winshine WS-53404-1.
[4]	Litz Wire: 125/#38 Single Coated, Unserved.
[5]	Litz Wire: 125/#40 Single Coated, Served.
[6]	Tape: Polyester Film, 3M 1350F-1 or equivalent, 10.0 mm wide.
[7]	Varnish: Dolph BC-359, or equivalent.

7.1.4 **Build Diagram**

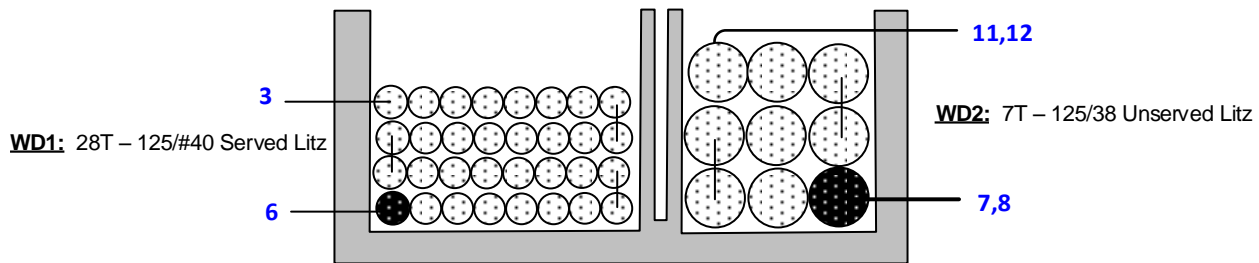

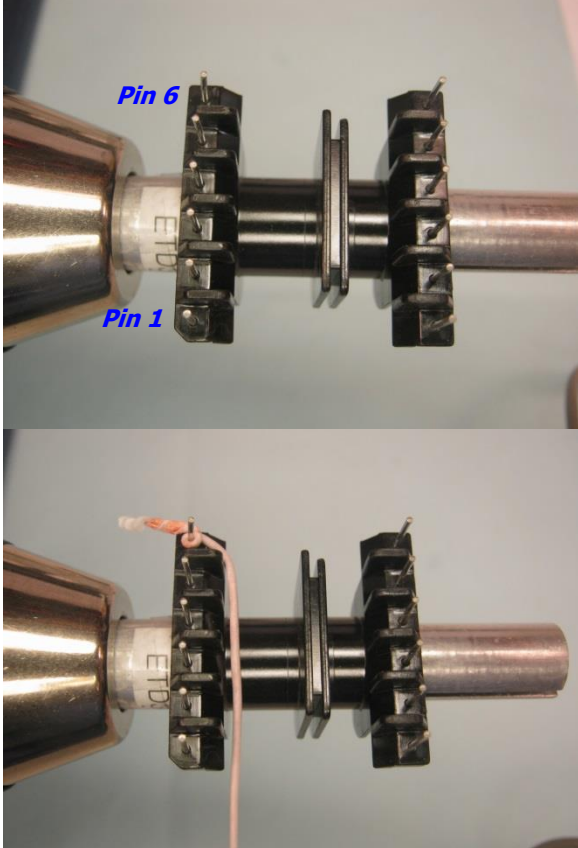


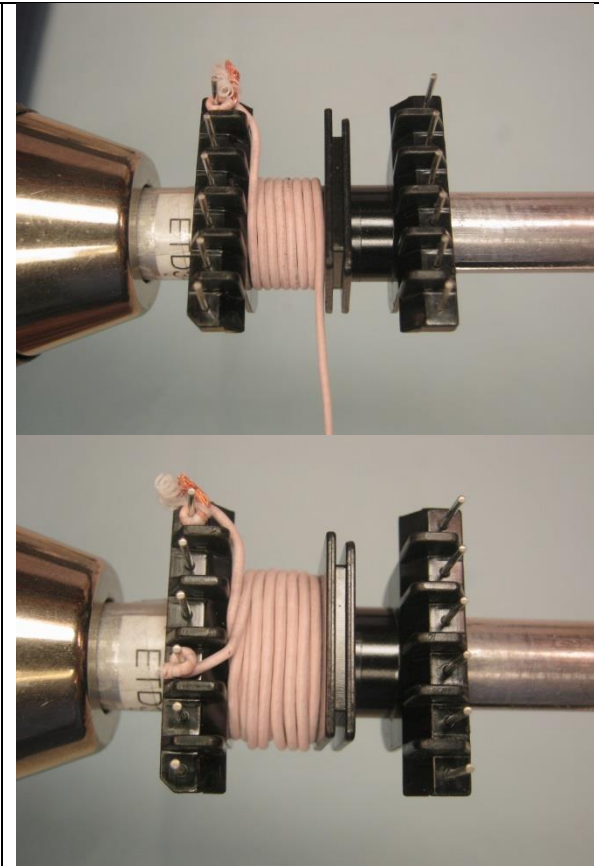
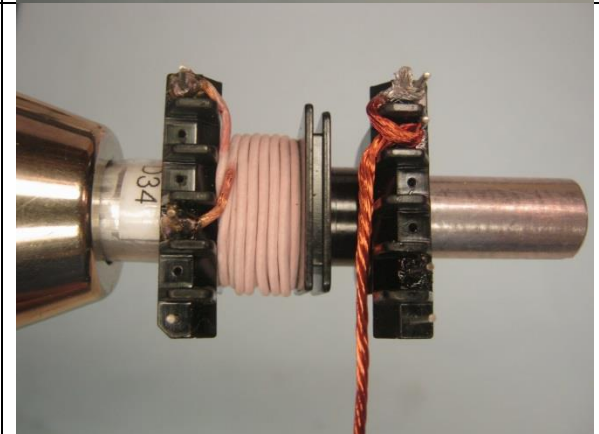
Figure 11 – LLC Transformer Build Diagram.

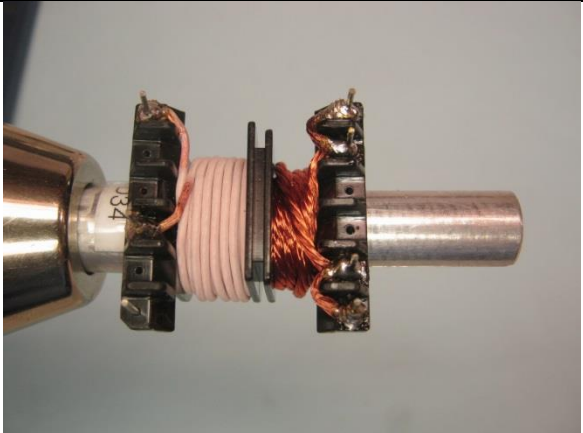

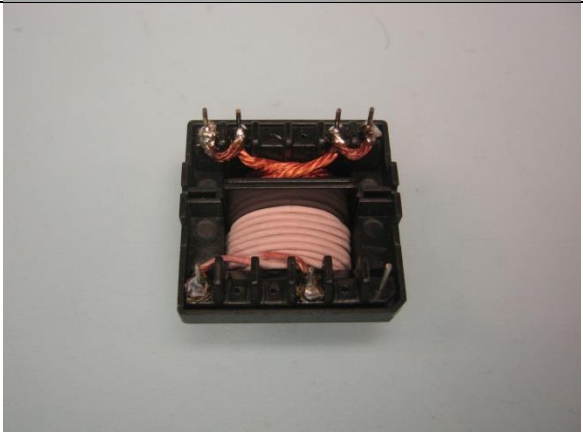
7.1.5 **Winding Instructions**

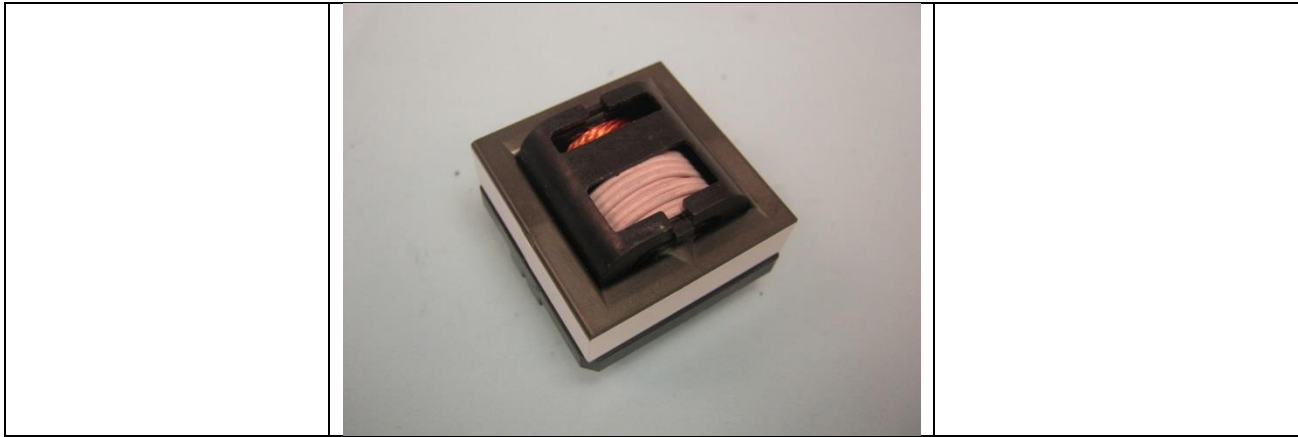
Secondary Wire Preparation	Prepare 1 strand of wire Item [4] 16" length, tin ends.
WD1 (Primary)	Place the bobbin Item [2] on the mandrel with larger chamber on the left side. Note: chamber used for primary winding is wider than chamber used for secondary. Pins 1-6 will be on left side. Starting on pin 6, wind 26 turns of served Litz wire Item [5] in ~4 layers, and finish on pin 3.
WD2 (Secondary)	Using unserved Litz assembly prepared in step 1, start on pins 7,8. Tightly wind 7 turns in secondary (right-hand) chamber, finish on pins 11, 12.
Bobbin Cover	Slide bobbin cover Item [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.
Finish	Remove pins 2,4,5,9, and 10 of bobbin. Grind core halves Item [1] for specified inductance. Assemble and secure core halves using circumferential turn of tape Item [6] as shown. Dip varnish Item [7].

7.1.6 **Winding Illustrations**

<p>Secondary Wire Preparation</p>		<p>Prepare 1 strand of wire Item [4] 16" length, tin ends.</p>
<p>WD1 (Primary)</p>		<p>Place the bobbin Item [2] on the mandrel with larger chamber on the left side. Note: chamber used for primary winding is wider than chamber used for secondary. Pins 1-6 will be on left side Starting on pin 6, wind 26 turns of served Litz wire Item [5] in ~ 4 layers, and finish on pin 3.</p>

		
<p>WD2 (Secondary)</p>		<p>Using unserved Litz assembly prepared in step 1, start on pins 7,8. Tightly wind 7 turns in secondary (right-hand) chamber, finish on pins 11, 12.</p>

		
<p>Bobbin Cover</p>		<p>Slide bobbin cover Item [3] into grooves in bobbin flanges as shown. Make sure cover is securely seated.</p>
<p>Finish</p>		<p>Remove pins 2,4,5,9, and 10 of bobbin. Grind core halves Item [1] for specified inductance. Assemble and secure core halves using circumferential turn of tape Item [6] as shown. Dip varnish Item [7].</p>



7.2 Standby Transformer (T2) Specification

7.2.1 Electrical Diagram

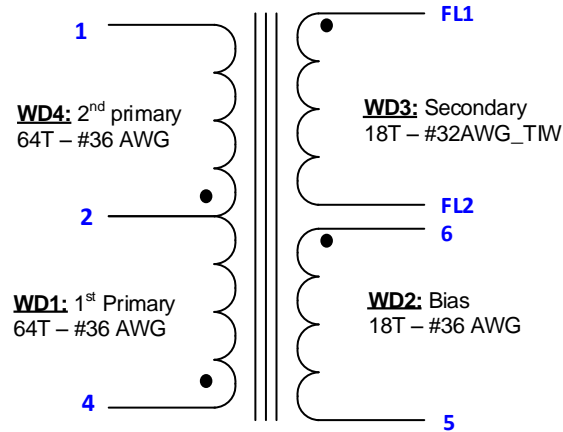


Figure 12 – Transformer Electrical Diagram.

7.2.2 Electrical Specifications

Electrical Strength	1 second, 60 Hz, from pins 1-4 to FL1-2	3000 V
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz, 0.4 V _{RMS} .	1.5 mH ±10%
Resonant Frequency	Pins 1-4, all other windings open	600 kHz (Min.)
Primary Leakage Inductance	Pins 1-4, with pins 5-8, FL1,FL2 shorted, measured at 100 kHz, 0.4 V _{RMS} .	20 μH (Max.)

7.2.3 Material List

Item	Description
[1]	Core: EE10, TDK PC40 material, (PI#: 99-00037-00) or equivalent. Gap for inductance coefficient (A_L) of 92 nH/T ²
[2]	Bobbin: EE10, vertical, 8 pins (4/4). TDK BE10-118CPSFR, Taiwan Shulin TF-10 (PI#: 25-00877-00); or equivalent.
[3]	Tape: Polyester film, 3M 1350F-1 or equivalent, 6.5 mm wide.
[4]	Wire: Magnet #36 AWG, solderable double coated.
[5]	Wire: Triple Insulated, Furukawa TEX-E or equivalent, #32 AWG.
[6]	Transformer Varnish, Dolph BC-359 or equivalent.

7.2.4 **Build Diagram**

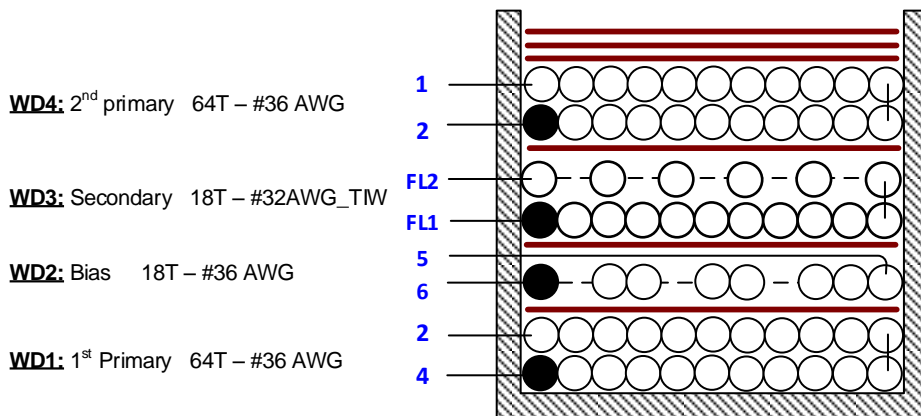
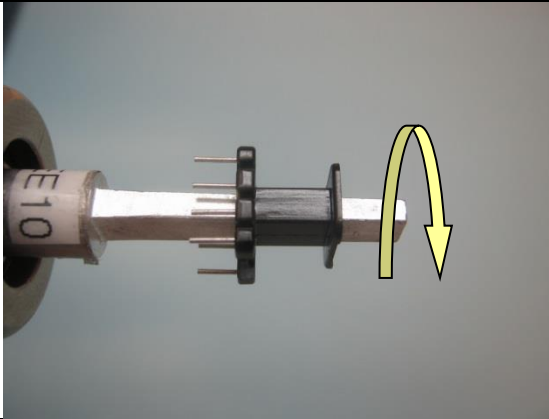
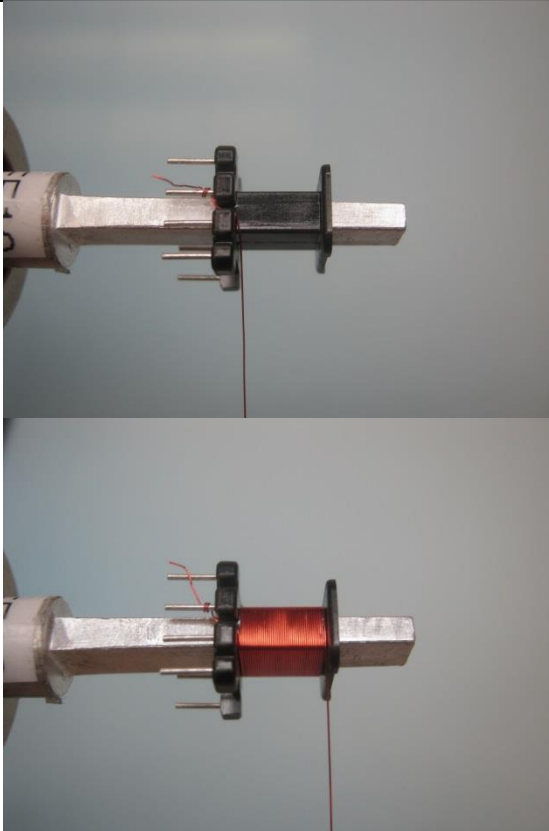


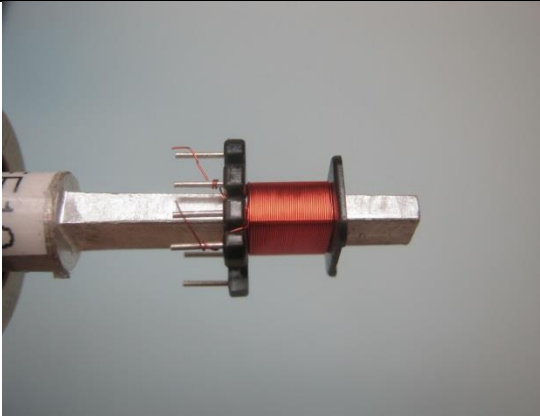

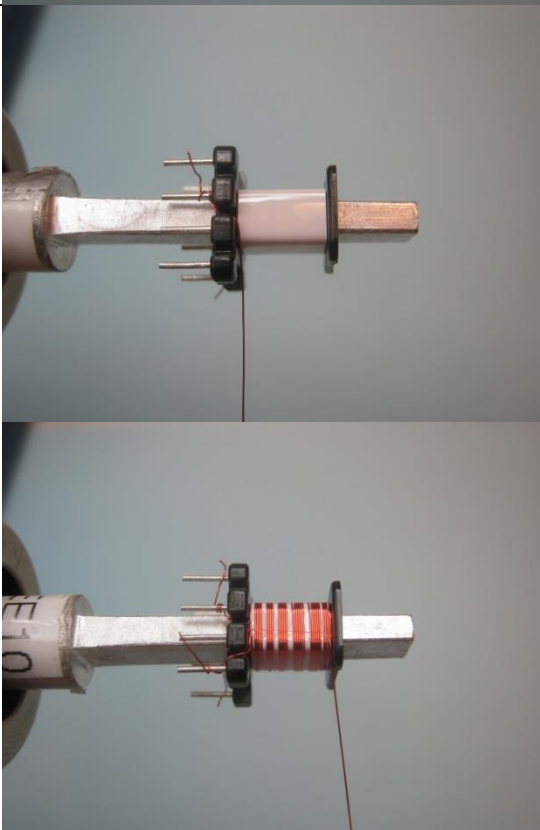
Figure 13 – Transformer Build Diagram.

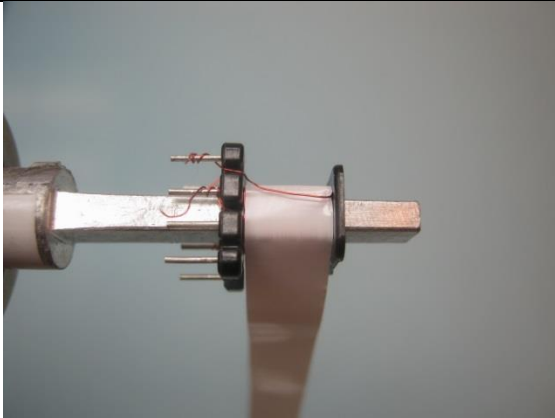
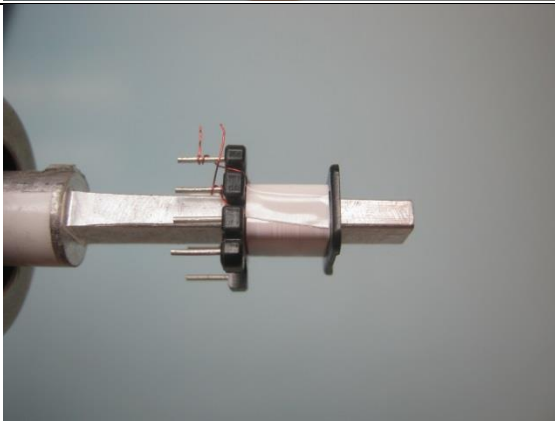
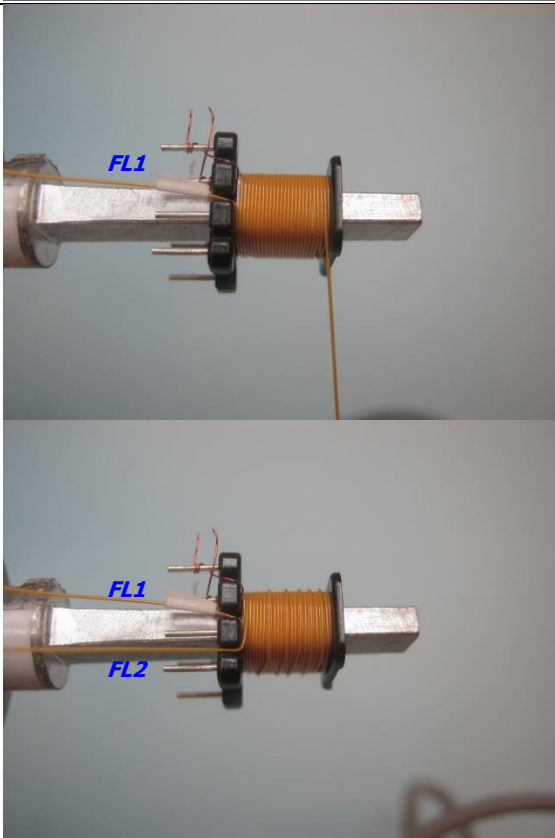
7.2.5 **Winding Instructions**

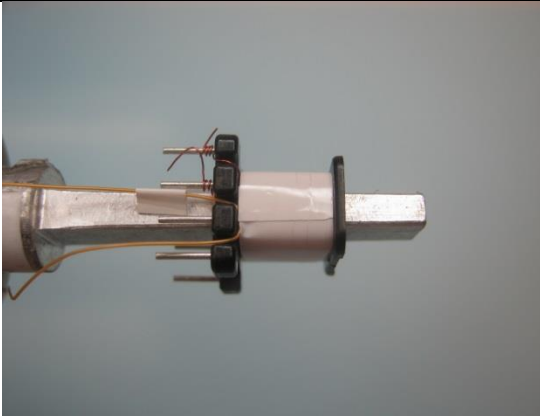
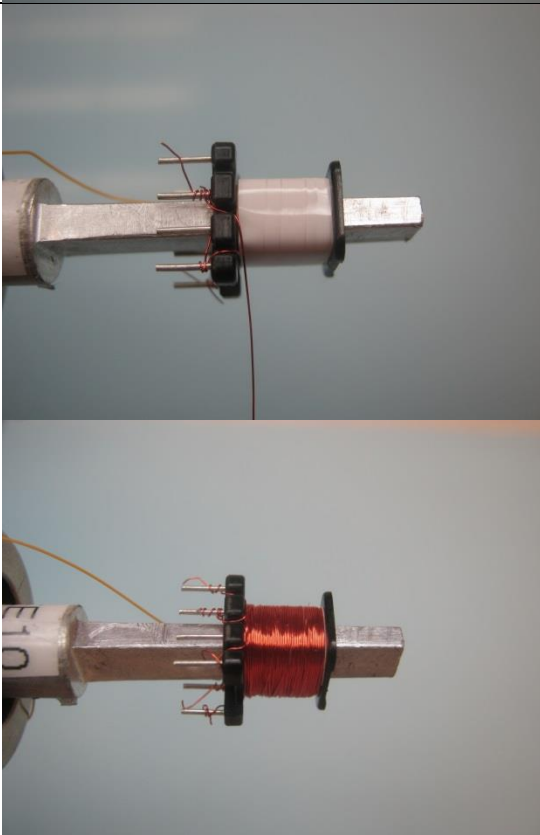
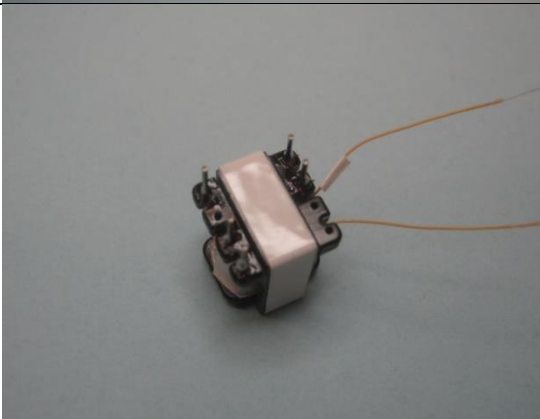
General Note	For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is clockwise.
WD1: 1st Primary	Starting at pin 4, wind 64 turns of wire Item [4] in 2 layers. Finish at pin 2.
Insulation	Use 1 layer of tape Item [3] for insulation.
WD2: Bias	Starting at pin 6, wind 18 turns of wire Item [4] in one layer. Finish at pin 5.
Insulation	Use 1 layer of tape Item [3] for insulation.
WD3: Secondary	Using wire Item [5], leave ~ 1" floating, and mark as FL1 for start lead. Wind 18 turns and also leave ~1" for end lead and mark as FL2.
Insulation	Use 1 layer of tape Item [3] for insulation.
WD4: 2nd Primary	Starting at pin 2, wind 64 turns of wire Item [4] in ~2 layers. Finish at Pin 1.
Insulation	Use 3 layers of tape Item [3] to secure the windings.
Assembly	Grind core halves for specified primary inductance, and secure core halves with tape. Remove pins 3, 7, 8. Dip varnish Item [6].

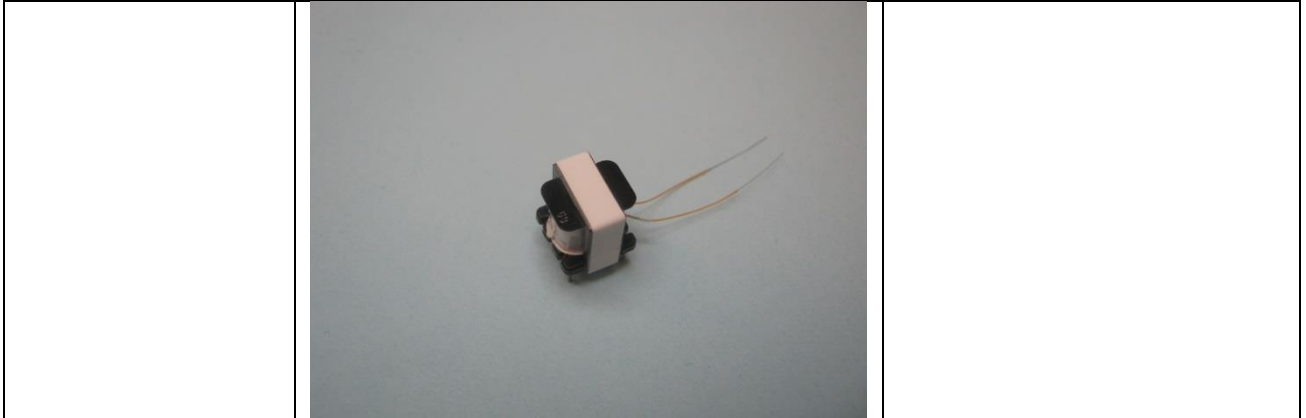
7.2.6 **Transformer Illustrations**

<p>General Note</p>		<p>For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side (see illustration). Winding direction as shown is clockwise.</p>
<p>WD1: 1st Primary</p>		<p>Starting at pin 4, wind 64 turns of wire Item [4] in 2 layers. Finish at pin 2.</p>

		
<p>Insulation</p>		<p>Use 1 layer of tape Item [3] for insulation.</p>
<p>WD2: Bias</p>		<p>Starting at pin 6, wind 18 turns of wire Item [4] in one layer. Finish at pin 5.</p>

		
<p>Insulation</p>		<p>Use 1 layer of tape Item [3] for insulation.</p>
<p>WD3: Secondary</p>		<p>Using wire Item [5], leave ~1" floating, and mark as FL1 for start lead. Wind 18 turns and also leave ~1" for end lead and mark as FL2.</p>

<p>Insulation</p>		<p>Use 1 layer of tape Item [3] for insulation.</p>
<p>WD4: 2nd Primary</p>		<p>Starting at pin 2, wind 64 turns of wire Item [4] in ~2 layers. Finish at pin 1.</p>
<p>Assembly</p>		<p>Grind core halves for specified primary inductance, and secure core halves with tape. Remove pins 3, 7, 8. Dip varnish Item [6].</p>



8 LLC Transformer Design Spreadsheet

HiperLCS_042413; Rev.1.3; Copyright Power Integrations 2013	INPUTS	INFO	OUTPUTS	UNITS	HiperLCS_042413_Rev1-3.xls; HiperLCS Half-Bridge, Continuous mode LLC Resonant Converter Design Spreadsheet
Enter Input Parameters					
Vbulk_nom	322		322	V	Nominal LLC input voltage
Vbrownout			237	V	Brownout threshold voltage. HiperLCS will shut down if voltage drops below this value. Allowable value is between 65% and 76% of Vbulk_nom. Set to 65% for max holdup time
Vbrownin			299	V	Start-up threshold on bulk capacitor
VOV_shut			394	V	OV protection on bulk voltage
VOV_restart			380	V	Restart voltage after OV protection.
CBULK	180.00		180	uF	Minimum value of bulk cap to meet holdup time requirement; Adjust holdup time and Vbrownout to change bulk cap value
tHOLDUP			17.0	ms	Bulk capacitor hold up time
Enter LLC (secondary) outputs					The spreadsheet assumes AC stacking of the secondaries
VO1	48.00		48.0	V	Main Output Voltage. Spreadsheet assumes that this is the regulated output
IO1	5.00		5.0	A	Main output maximum current
VD1	1.00		1.00	V	Forward voltage of diode in Main output
PO1			240	W	Output Power from first LLC output
VO2			0.0	V	Second Output Voltage
IO2			0.0	A	Second output current
VD2			0.70	V	Forward voltage of diode used in second output
PO2			0.00	W	Output Power from second LLC output
P_LLC			240	W	Specified LLC output power
LCS Device Selection					
Device	LCS708	Warning	LCS708		!!! Warning. Device may be too large. Select smaller device
RDS-ON (MAX)			0.46	ohms	RDS-ON (max) of selected device
Coss			749	pF	Equivalent Coss of selected device
Cpri			40	pF	Stray Capacitance at transformer primary
Pcond_loss			2.9	W	Conduction loss at nominal line and full load
Tmax-hs			90	deg C	Maximum heatsink temperature
Theta J-HS			8.0	deg C/W	Thermal resistance junction to heatsink (with grease and no insulator)
Expected Junction temperature			113	deg C	Expected Junction temperature
Ta max			50	deg C	Expected max ambient temperature
Theta HS-A			14	deg C/W	Required thermal resistance heatsink to ambient
LLC Resonant Parameter and Transformer Calculations (generates red curve)					
Vres_target	320.00		320	V	Desired Input voltage at which power train operates at resonance. If greater than Vbulk_nom, LLC operates below resonance at VBULK.
Po			245	W	LLC output power including diode loss
Vo			49.00	V	Main Output voltage (includes diode drop) for calculating Nsec and turns ratio
f_target	120.00		120	kHz	Desired switching frequency at Vbulk_nom. 66 kHz to 300 kHz, recommended 180-250 kHz
Lpar			119	uH	Parallel inductance. (Lpar = Lopen - Lres for integrated transformer; Lpar = Lmag for non-integrated low-leakage transformer)
Lpri	160.00		160	uH	Primary open circuit inductance for integrated transformer; for low-leakage transformer it is sum of primary inductance and series inductor. If left blank, auto-calculation shows value necessary for slight loss of ZVS at ~80% of Vnom
Lres	41.00		41.0	uH	Series inductance or primary leakage inductance of



					integrated transformer; if left blank auto-calculation is for K=4
Kratio			2.9		Ratio of Lpar to Lres. Maintain value of K such that $2.1 < K < 11$. Preferred Lres is such that $K < 7$.
Cres	39.00		39.0	nF	Series resonant capacitor. Red background cells produce red graph. If Lpar, Lres, Cres, and n_RATIO_red_graph are left blank, they will be auto-calculated
Lsec			11.598	uH	Secondary side inductance of one phase of main output; measure and enter value, or adjust value until f_predicted matches what is measured ;
m			50	%	Leakage distribution factor (primary to secondary). >50% signifies most of the leakage is in primary side. Gap physically under secondary yields >50%, requiring fewer primary turns.
n_eq			3.20		Turns ratio of LLC equivalent circuit ideal transformer
Npri	26.0		26.0		Primary number of turns; if input is blank, default value is auto-calculation so that f_predicted = f_target and m=50%
Nsec	7.0		7.0		Secondary number of turns (each phase of Main output). Default value is estimate to maintain $BAC \leq 200$ mT, using selected core (below)
f_predicted			127	kHz	Expected frequency at nominal input voltage and full load; Heavily influenced by n_eq and primary turns
f_res			126	kHz	Series resonant frequency (defined by series inductance Lres and C)
f_brownout			97	kHz	Expected switching frequency at Vbrownout, full load. Set HiperLCS minimum frequency to this value.
f_par			64	kHz	Parallel resonant frequency (defined by Lpar + Lres and C)
f_inversion			79	kHz	LLC full load gain inversion frequency. Operation below this frequency results in operation in gain inversion region.
Vinversion			155	V	LLC full load gain inversion point input voltage
Vres_expected			314	V	Expected value of input voltage at which LLC operates at resonance.
RMS Currents and Voltages					
IRMS_LLC_Primary			2.50	A	Primary winding RMS current at full load, Vbulk_nom and f_predicted
Winding 1 (Lower secondary Voltage) RMS current			4.0	A	Winding 1 (Lower secondary Voltage) RMS current
Lower Secondary Voltage Capacitor RMS current			2.6	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			0.0	A	Winding 2 (Higher secondary Voltage) RMS current
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Cres_Vrms			81	V	Resonant capacitor AC RMS Voltage at full load and nominal input voltage
Virtual Transformer Trial - (generates blue curve)					
New primary turns			26.0		Trial transformer primary turns; default value is from resonant section
New secondary turns			7.0		Trial transformer secondary turns; default value is from resonant section
New Lpri			160	uH	Trial transformer open circuit inductance; default value is from resonant section
New Cres			39.0	nF	Trial value of series capacitor (if left blank calculated value chosen so f_res same as in main

					resonant section above
New estimated Lres			41.0	uH	Trial transformer estimated Lres
New estimated Lpar			119	uH	Estimated value of Lpar for trial transformer
New estimated Lsec			11.598	uH	Estimated value of secondary leakage inductance
New Kratio			2.9		Ratio of Lpar to Lres for trial transformer
New equivalent circuit transformer turns ratio			3.20		Estimated effective transformer turns ratio
V powertrain inversion new			155	V	Input voltage at LLC full load gain inversion point
f_res_trial			126	kHz	New Series resonant frequency
f_predicted_trial			127	kHz	New nominal operating frequency
IRMS_LLC_Primary			2.50	A	Primary winding RMS current at full load and nominal input voltage (Vbulk) and f_predicted_trial
Winding 1 (Lower secondary Voltage) RMS current			4.1	A	RMS current through Output 1 winding, assuming half sinusoidal waveshape
Lower Secondary Voltage Capacitor RMS current			2.8	A	Lower Secondary Voltage Capacitor RMS current
Winding 2 (Higher secondary Voltage) RMS current			4.1	A	RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Higher Secondary Voltage Capacitor RMS current			0.0	A	Higher Secondary Voltage Capacitor RMS current
Vres_expected_trial			314	V	Expected value of input voltage at which LLC operates at resonance.
Transformer Core Calculations (Calculates From Resonant Parameter Section)					
Transformer Core	PQ20/20		PQ20/20		Transformer Core
Ae	0.97		0.97	cm ²	Enter transformer core cross-sectional area
Ve	7.63		7.63	cm ³	Enter the volume of core
Aw	122.00		122.0	mm ²	Area of window
Bw	20.90		20.9	mm	Total Width of Bobbin
Loss density			200.0	mW/cm ³	Enter the loss per unit volume at the switching frequency and BAC (Units same as kW/m ³)
MLT			4.4	cm	Mean length per turn
Nchambers			2		Number of Bobbin chambers
Wsep			3.0	mm	Winding separator distance (will result in loss of winding area)
Ploss			1.5	W	Estimated core loss
Bpkfmin			186	mT	First Quadrant peak flux density at minimum frequency.
BAC			285	mT	AC peak to peak flux density (calculated at f_predicted, Vbulk at full load)
Primary Winding					
Npri			26.0		Number of primary turns; determined in LLC resonant section
Primary gauge	40		40	AWG	Individual wire strand gauge used for primary winding
Equivalent Primary Metric Wire gauge			0.080	mm	Equivalent diameter of wire in metric units
Primary litz strands	125		125		Number of strands in Litz wire; for non-litz primary winding, set to 1
Primary Winding Allocation Factor			50	%	Primary window allocation factor - percentage of winding space allocated to primary
AW_P			52	mm ²	Winding window area for primary
Fill Factor			52%	%	% Fill factor for primary winding (typical max fill is 60%)
Resistivity_25 C_Primary			29.83	m-ohm/m	Resistivity in milli-ohms per meter
Primary DCR 25 C			34.13	m-ohm	Estimated resistance at 25 C
Primary DCR 100 C			45.73	m-ohm	Estimated resistance at 100 C (approximately 33% higher than at 25 C)
Primary RMS current			2.50	A	Measured RMS current through the primary winding
ACR_Trf_Primary			127.39	m-ohm	Measured AC resistance (at 100 kHz, room



					temperature), multiply by 1.33 to approximate 100 C winding temperature
Primary copper loss		0.80	W		Total primary winding copper loss at 85 C
Primary Layers		3.37			Number of layers in primary Winding
Secondary Winding 1 (Lower secondary voltage OR Single output)					Note - Power loss calculations are for each winding half of secondary
Output Voltage		48.00	V		Output Voltage (assumes AC stacked windings)
Sec 1 Turns		7.00			Secondary winding turns (each phase)
Sec 1 RMS current (total, AC+DC)		4.0	A		RMS current through Output 1 winding, assuming half sinusoidal waveshape
Winding current (DC component)		2.50	A		DC component of winding current
Winding current (AC RMS component)		3.11	A		AC component of winding current
Sec 1 Wire gauge		38	AWG		Individual wire strand gauge used for secondary winding
Equivalent secondary 1 Metric Wire gauge		0.100	mm		Equivalent diameter of wire in metric units
Sec 1 litz strands	125	125			Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec1		18.76	m-ohm/m		Resistivity in milli-ohms per meter
DCR_25C_Sec1		5.78	m-ohm		Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec1		7.74	m-ohm		Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1		0.39	W		Estimated Power loss due to DC resistance (both secondary phases)
ACR_Sec1		8.17	m-ohm		Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec1		0.16	W		Estimated AC copper loss (both secondary phases)
Total winding 1 Copper Losses		0.55	W		Total (AC + DC) winding copper loss for both secondary phases
Capacitor RMS current		2.6	A		Output capacitor RMS current
Co1		4.2	uF		Secondary 1 output capacitor
Capacitor ripple voltage		3.0	%		Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current		4.0	A		Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 1 Layers		1.13			Number of layers in secondary 1 Winding
Secondary Winding 2 (Higher secondary voltage)					Note - Power loss calculations are for each winding half of secondary
Output Voltage		0.00	V		Output Voltage (assumes AC stacked windings)
Sec 2 Turns		0.00			Secondary winding turns (each phase) AC stacked on top of secondary winding 1
Sec 2 RMS current (total, AC+DC)		4.0	A		RMS current through Output 2 winding; Output 1 winding is AC stacked on top of Output 2 winding
Winding current (DC component)		0.0	A		DC component of winding current
Winding current (AC RMS component)		0.0	A		AC component of winding current
Sec 2 Wire gauge		38	AWG		Individual wire strand gauge used for secondary winding
Equivalent secondary 2 Metric Wire gauge		0.100	mm		Equivalent diameter of wire in metric units
Sec 2 litz strands		0			Number of strands used in Litz wire; for non-litz non-integrated transformer set to 1
Resistivity_25 C_sec2		23453.09	m-ohm/m		Resistivity in milli-ohms per meter
Transformer Secondary MLT		4.40	cm		Mean length per turn

DCR_25C_Sec2			0.00	m-ohm	Estimated resistance per phase at 25 C (for reference)
DCR_100C_Sec2			0.00	m-ohm	Estimated resistance per phase at 100 C (approximately 33% higher than at 25 C)
DCR_Ploss_Sec1			0.00	W	Estimated Power loss due to DC resistance (both secondary halves)
ACR_Sec2			0.00	m-ohm	Measured AC resistance per phase (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature. Default value of ACR is twice the DCR value at 100 C
ACR_Ploss_Sec2			0.00	W	Estimated AC copper loss (both secondary halves)
Total winding 2 Copper Losses			0.00	W	Total (AC + DC) winding copper loss for both secondary halves
Capacitor RMS current			0.0	A	Output capacitor RMS current
Co2			N/A	uF	Secondary 2 output capacitor
Capacitor ripple voltage			N/A	%	Peak to Peak ripple voltage on secondary 1 output capacitor
Output rectifier RMS Current			0.0	A	Schottky losses are a stronger function of load DC current. Sync Rectifier losses are a function of RMS current
Secondary 2 Layers			1.00		Number of layers in secondary 2 Winding
Transformer Loss Calculations					Does not include fringing flux loss from gap
Primary copper loss (from Primary section)			0.80	W	Total primary winding copper loss at 85 C
Secondary copper Loss			0.55	W	Total copper loss in secondary winding
Transformer total copper loss			1.34	W	Total copper loss in transformer (primary + secondary)
AW_S			52.24	mm ²	Area of window for secondary winding
Secondary Fill Factor			44%	%	% Fill factor for secondary windings; typical max fill is 60% for served and 75% for unserved Litz
Signal Pins Resistor Values					
f_min			97	kHz	Minimum frequency when optocoupler is cut-off. Only change this variable based on actual bench measurements
Dead Time			320	ns	Dead time
Burst Mode	1		1		Select Burst Mode: 1, 2, and 3 have hysteresis and have different frequency thresholds
f_max			847	kHz	Max internal clock frequency, dependent on dead-time setting. Is also start-up frequency
f_burst_start			382	kHz	Lower threshold frequency of burst mode, provides hysteresis. This is switching frequency at restart after a bursting off-period
f_burst_stop			437	kHz	Upper threshold frequency of burst mode; This is switching frequency at which a bursting off-period stops
DT/BF pin upper divider resistor			6.79	k-ohms	Resistor from DT/BF pin to VREF pin
DT/BF pin lower divider resistor			129	k-ohms	Resistor from DT/BF pin to G pin
Rstart			5.79	k-ohms	Start-up resistor - resistor in series with soft-start capacitor; equivalent resistance from FB to VREF pins at startup. Use default value unless additional start-up delay is desired.
Start up delay			0.0	ms	Start-up delay; delay before switching begins. Reduce R_START to increase delay
Rfmin			80.8	k-ohms	Resistor from VREF pin to FB pin, to set min operating frequency; This resistor plus Rstart determine f_MIN. Includes 7% HiperLCS frequency tolerance to ensure f_min is below f_brownout
C_softstart			0.33	uF	Softstart capacitor. Recommended values are between 0.1 uF and 0.47 uF
Ropto			1.2	k-ohms	Resistor in series with opto emitter
OV/UV pin lower resistor			22.0	k-ohm	Lower resistor in OV/UV pin divider



OV/UV pin upper resistor			2.72	M-ohm	Total upper resistance in OV/UV pin divider
LLC Capacitive Divider Current Sense Circuit					
Slow current limit	10.50		10.50	A	8-cycle current limit - check positive half-cycles during brownout and startup
Fast current limit			18.90	A	1-cycle current limit - check positive half-cycles during startup
LLC sense capacitor			47	pF	HV sense capacitor, forms current divider with main resonant capacitor
RLLC sense resistor			39.6	ohms	LLC current sense resistor, senses current in sense capacitor
IS pin current limit resistor			220	ohms	Limits current from sense resistor into IS pin when voltage on sense R is < -0.5V
IS pin noise filter capacitor			1.0	nF	IS pin bypass capacitor; forms a pole with IS pin current limit capacitor
IS pin noise filter pole frequency			724	kHz	This pole attenuates IS pin signal
Loss Budget					
LCS device Conduction loss			2.9	W	Conduction loss at nominal line and full load
Output diode Loss			5.0	W	Estimated diode losses
Transformer estimated total copper loss			1.34	W	Total copper loss in transformer (primary + secondary)
Transformer estimated total core loss			1.5	W	Estimated core loss
Total transformer losses			2.9	W	Total transformer losses
Total estimated losses			10.8	W	Total losses in LLC stage
Estimated Efficiency			96%	%	Estimated efficiency
PIN			251	W	LLC input power
Secondary Turns and Voltage Centering Calculator					
This is to help you choose the secondary turns - Outputs not connected to any other part of spreadsheet					
V1			48.00	V	Target regulated output voltage Vo1. Change to see effect on slave output
V1d1			1.00	V	Diode drop voltage for Vo1
N1			8.00		Total number of turns for Vo1
V1_Actual			48.00	V	Expected output
V2			0.00	V	Target output voltage Vo2
V2d2			0.70	V	Diode drop voltage for Vo2
N2			1.00		Total number of turns for Vo2
V2_Actual			5.43	V	Expected output voltage
Separate Series Inductor (For Non-Integrated Transformer Only)					
Not applicable if using integrated magnetics - not connected to any other part of spreadsheet					
Lsep			41.00	uH	Desired inductance of separate inductor
Ae_Ind			0.53	cm ²	Inductor core cross-sectional area
Inductor turns			28		Number of primary turns
BP_fnom			105	mT	AC flux for core loss calculations (at f_predicted and full load)
Expected peak primary current			10.5	A	Expected peak primary current
BP_fmin			293	mT	Peak flux density, calculated at minimum frequency fmin
Inductor Litz gauge			41	AWG	Individual wire strand gauge used for primary winding
Equivalent Inductor Metric Wire gauge			0.070	mm	Equivalent diameter of wire in metric units
Inductor litz strands			125.00		Number of strands used in Litz wire
Inductor parallel wires			1		Number of parallel individual wires to make up Litz wire
Resistivity_25_C_Sep_Ind			37.6	m-ohm/m	Resistivity in milli-ohms per meter
Inductor MLT			7.00	cm	Mean length per turn
Inductor DCR 25 C			73.7	m-ohm	Estimated resistance at 25 C (for reference)
Inductor DCR 100 C			98.8	m-ohm	Estimated resistance at 100 C (approximately 33%)

					higher than at 25 C)
ACR_Sep_Inductor			158.1	m-ohm	Measured AC resistance (at 100 kHz, room temperature), multiply by 1.33 to approximate 100 C winding temperature
Inductor copper loss			0.99	W	Total primary winding copper loss at 85 C
Feedback section					
VMAIN	Auto		48.0		Output voltage rail that optocoupler LED is connected to
ITL431_BIAS			1.0	mA	Minimum operating current in TL431 cathode
VF			1.0	V	Typical Optocoupler LED forward voltage at IOPTO_BJTMAX (max current)
VCE_SAT			0.3	V	Optocoupler transistor saturation voltage
CTR_MIN			0.8		Optocoupler minimum CTR at VCE_SAT and at IOPTO_BJT_MAX
VTL431_SAT			2.5	V	TL431 minimum cathode voltage when saturated
RLED_SHUNT			1.0	k-ohms	Resistor across optocoupler LED to ensure minimum TL431 bias current is met
ROPTO_LOAD			4.70	k-ohms	Resistor from optocoupler emitter to ground, sets load current
IFMAX			347.08	uA	FB pin current when switching at FMAX (e.g. startup)
IOPTO_BJT_MAX			0.97	mA	Optocoupler transistor maximum current - when bursting at FMAX (e.g. startup)
RLED_SERIES_MAX			18.10	k-ohms	Maximum value of gain setting resistor, in series with optocoupler LED, to ensure optocoupler can deliver IOPTO_BJT_MAX. Includes -10% tolerance factor.

Note: Device Warning: LCS708 selected for improved thermal performance at low line.

9 Standby Transformer Design Spreadsheet

ACDC_LinkSwitch-TN_Flyback_042413; Rev.1.10; Copyright Power Integrations 2007	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitch-TN Flyback_042413; Copyright Power Integrations 2007
ENTER APPLICATION VARIABLES					
VACMIN	180			Volts	Minimum AC Input Voltage
VACMAX	264			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12.00			Volts	Output Voltage (main) (For CC designs enter upper CV tolerance limit)
IO	0.05			Amps	Power Supply Output Current (For CC designs enter upper CC tolerance limit)
CC Threshold Voltage	0.00			Volts	Voltage drop across sense resistor.
Output Cable Resistance	0.00		0.00	Ohms	Enter the resistance of the output cable (if used)
PO			0.60	Watts	Output Power (VO x IO + CC dissipation)
Feedback Type	OPTO		Opto		Choose 'BIAS' for Bias winding feedback and 'OPTO' for Optocoupler feedback from the 'Feedback Type' drop down box at the top of this spreadsheet
Add Bias Winding	YES		Yes		Choose 'YES' in the 'Bias Winding' drop down box at the top of this spreadsheet to add a Bias winding. Choose 'NO' to continue design without a Bias winding. Addition of Bias winding can lower no load consumption
n	0.80		0.8		Efficiency Estimate at output terminals.
Z			0.5		Loss Allocation Factor (suggest 0.5 for CC=0 V, 0.75 for CC=1 V)
tC	2.90			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	120.00			uFarads	Input Capacitance
Input Rectification Type	F		F		Choose H for Half Wave Rectifier and F for Full Wave Rectification from the 'Rectification' drop down box at the top of this spreadsheet
ENTER LinkSwitch-TN VARIABLES					
LinkSwitch-TN	LNK302		LNK302		User selection for LinkSwitch-TN. Ordering info - Suffix P/G indicates DIP 8 package; suffix D indicates SO8 package; second suffix N indicates lead free RoHS compliance
Chosen Device		LNK302			
ILIMITMIN			0.126	Amps	Minimum Current Limit
ILIMITMAX			0.146	Amps	Maximum Current Limit
fSmin			62000	Hertz	Minimum Device Switching Frequency
I ² fmin			984.312	A ² Hz	I ² f (product of current limit squared and frequency is trimmed for tighter tolerance)
VOR	90.00		90	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-TN on-state Drain to Source Voltage
VD			0.7	Volts	Output Winding Diode Forward Voltage Drop
KP			7.19		Ripple to Peak Current Ratio (0.6 < KP < 6.0).
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EE10		EE10		User-Selected transformer core
Core		EE10		P/N:	PC40EE10-Z
Bobbin		EE10_BOBBIN		P/N:	EE10_BOBBIN
AE			0.121	cm ²	Core Effective Cross Sectional Area
LE			2.61	cm	Core Effective Path Length
AL			850	nH/T ²	Ungapped Core Effective Inductance

BW			6.6	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	4.00		4		Number of Primary Layers
NS			18		Number of Secondary Turns
NB	18		18		Number of Bias winding turns
VB			12.70	Volts	Bias Winding voltage
PIVB			58	Volts	Bias Diode Maximum Peak Inverse Voltage
DC INPUT VOLTAGE PARAMETERS					
VMIN			254	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.05		Maximum Duty Cycle
IAVG			0.00	Amps	Average Primary Current
IP			0.13	Amps	Minimum Peak Primary Current
IR			0.13	Amps	Primary Ripple Current
IRMS			0.02	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1524	uHenries	Typical Primary Inductance. +/- 10%
LP_TOLERANCE			10	%	Primary inductance tolerance
NP			128		Primary Winding Number of Turns
ALG			94	nH/T^2	Gapped Core Effective Inductance
BM			1442	Gauss	Maximum Operating Flux Density, BM<1500 is recommended
BAC			721	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1459		Relative Permeability of Ungapped Core
LG			0.14	mm	Gap Length (Lg > 0.1 mm)
BWE			26.4	mm	Effective Bobbin Width
OD			0.21	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.16	mm	Bare conductor diameter
AWG			34	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			40	Cmils	Bare conductor effective area in circular mils
CMA		Info	2562	Cmils/Amp	!!! Info. Can decrease CMA < 500 (decrease L(primary layers),increase NS,use smaller Core)
TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			0.89	Amps	Peak Secondary Current
ISRMS			0.18	Amps	Secondary RMS Current
IRIPPLE			0.18	Amps	Output Capacitor RMS Ripple Current
CMS			37	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			34	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.16	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.37	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.10	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN			584	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS			65	Volts	Output Rectifier Maximum Peak Inverse Voltage
FEEDBACK COMPONENTS					



Recommended Bias Diode			1N4003 - 1N4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI. See LinkSwitch-TN Design Guide
R1			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-TN Design Guide
R2			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-TN Design Guide
TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			12.00	Volts	Main Output Voltage (if unused, defaults to single output design)
IO1			0.05	Amps	Output DC Current
PO1			0.60	Watts	Output Power
VD1			0.70	Volts	Output Diode Forward Voltage Drop
NS1			18.00		Output Winding Number of Turns
ISRMS1			0.18	Amps	Output Winding RMS Current
IRIPPLE1			0.18	Amps	Output Capacitor RMS Ripple Current
PIVS1			64.88	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diodes			SB180		Recommended Diodes for this output
Pre-Load Resistor			4	k-Ohms	Recommended value of pre-load resistor
CMS1			36.75	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			34.00	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.16	mm	Minimum Bare Conductor Diameter
ODS1			0.37	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.70	Volts	Output Diode Forward Voltage Drop
NS2			0.99		Output Winding Number of Turns
ISRMS2			0.00	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			2.91	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS2			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.70	Volts	Output Diode Forward Voltage Drop
NS3			0.99		Output Winding Number of Turns
ISRMS3			0.00	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			2.91	Volts	Output Rectifier Maximum Peak Inverse Voltage
Recommended Diode					Recommended Diodes for this output
CMS3			0.00	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)



DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			0.60	Watts	Total Output Power



10 Heat Sinks

10.1 Primary Heat Sink

10.1.1 Primary Heat Sink Sheet Metal

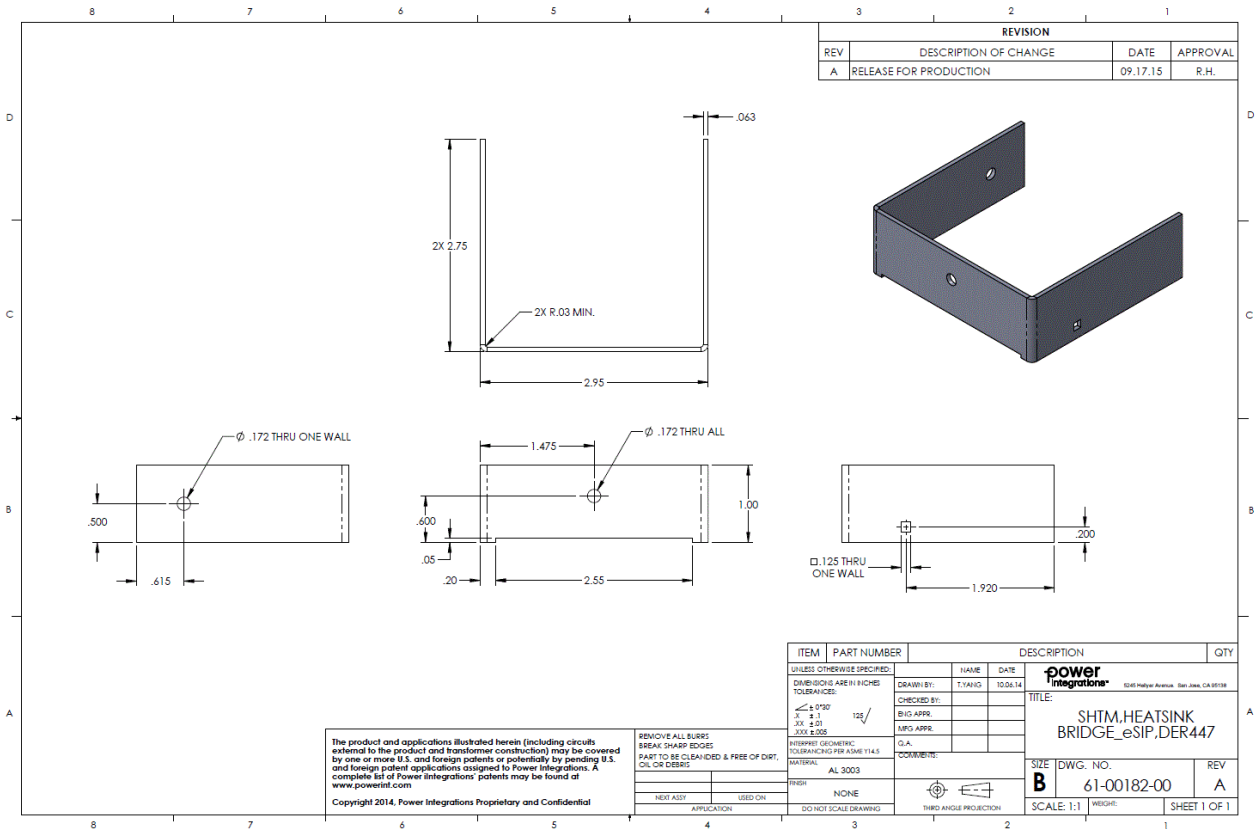


Figure 14 – Primary Heat Sink Sheet Metal Drawing.



10.1.2 **Primary Heat Sink with Fasteners**

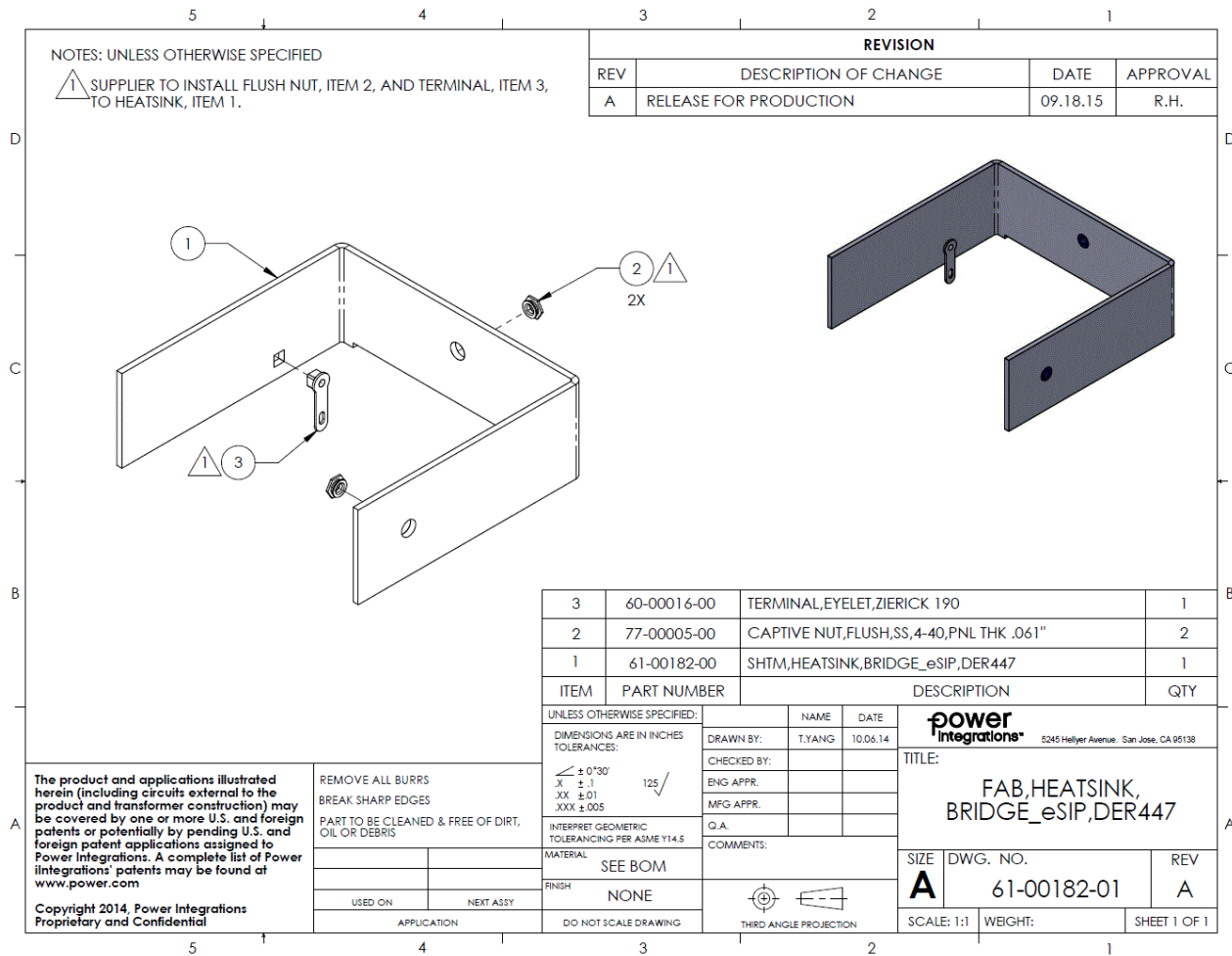


Figure 15 – Finished Primary Heat Sink Drawing with Installed Fasteners.

10.1.3 **Primary Heat Sink Assembly**

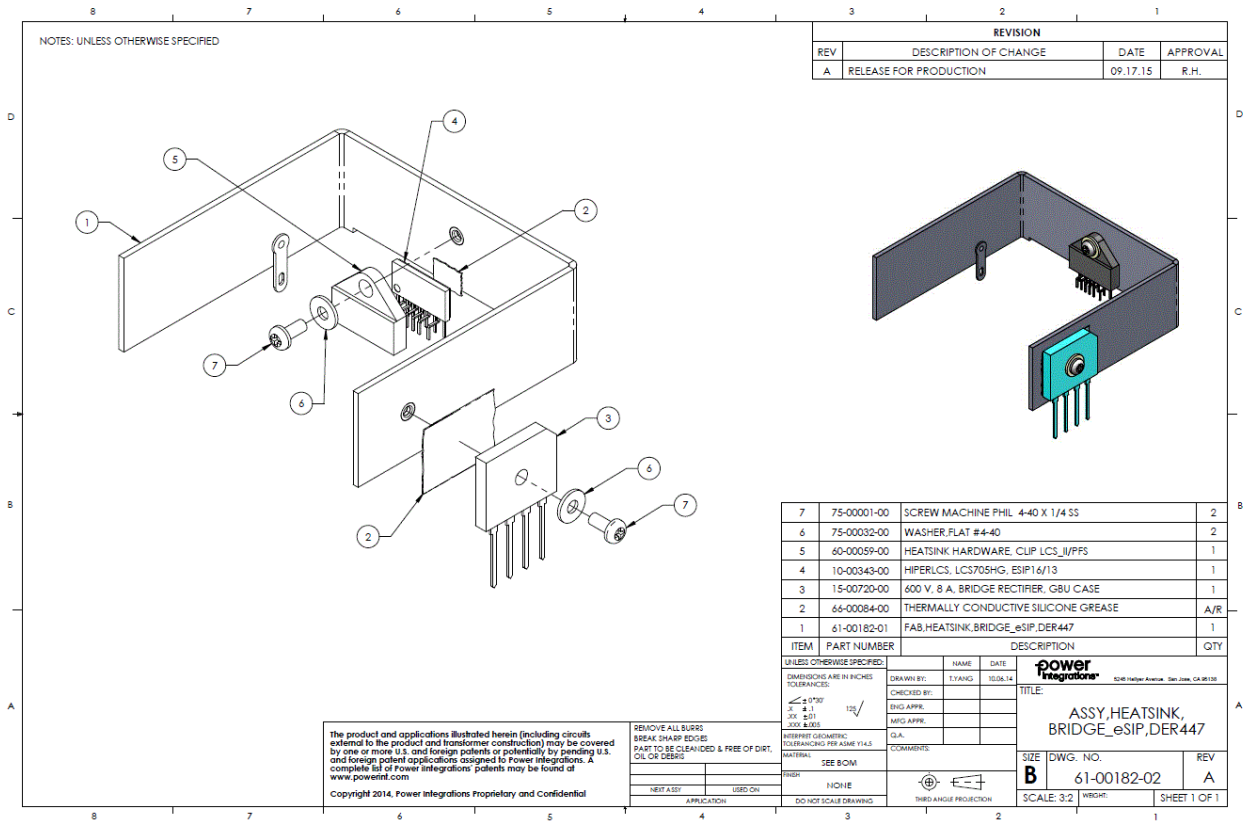


Figure 16 – Primary Heat Sink Assembly.



10.2 **Secondary Heat Sink**

10.2.1 **Secondary Heat Sink Sheet Metal**

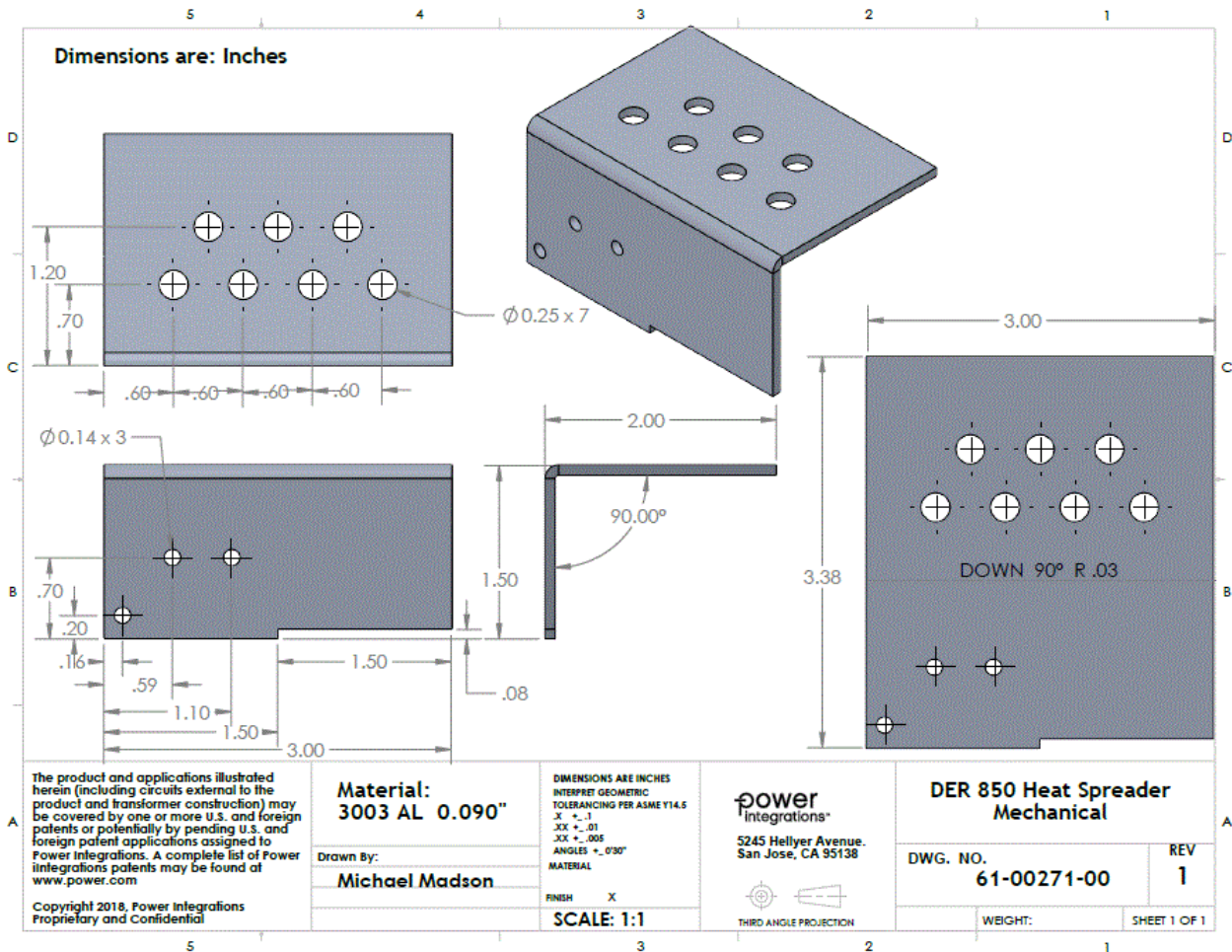


Figure 17 – Secondary Heat Sink Sheet Metal Drawing.

10.2.2 **Secondary Heat Sink with Fasteners**

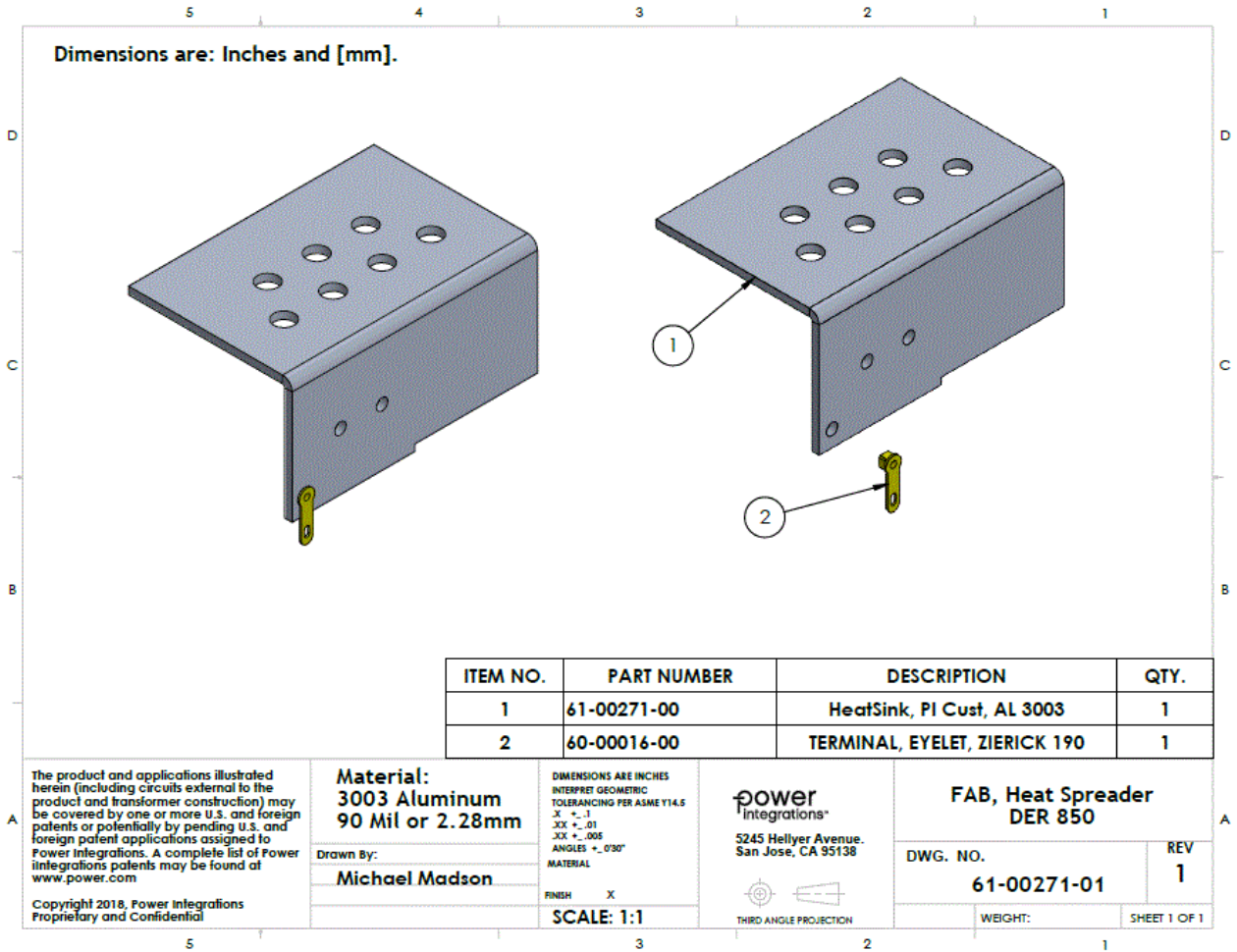


Figure 18 – Finished Secondary Heat Sink with Installed Fasteners.

10.2.3 **Secondary Heat Sink Assembly**

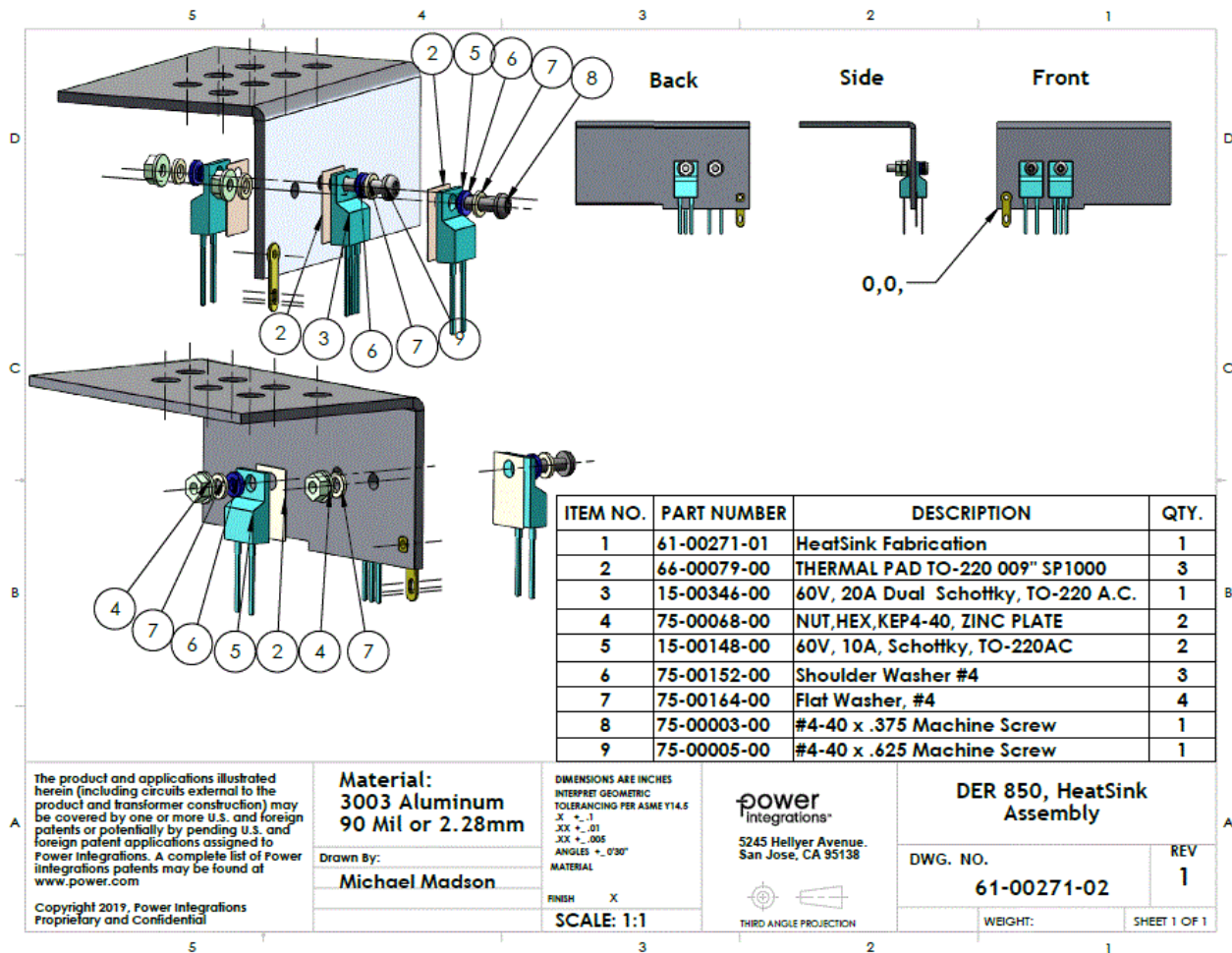


Figure 19 – Secondary Heat Sink Assembly.

11 Performance Data

All measurements were taken at room temperature and 50 Hz (input frequency) unless otherwise specified. Output voltage measurements were taken at the output connectors.

11.1 *Output Load Considerations for Testing a CV/CC Supply in Battery Charger Applications*

Since this power supply has a constant voltage/constant current output and normally operates in CC mode in its intended application (battery charging), some care must be taken in selecting the type/s of output load for testing.

The default setting for most electronic loads is constant current. This setting can be used in testing a CV/CC supply in the CV portion of its load range below the power supply current limit set point. Once the current limit of the DUT is reached, a constant current load will cause the output voltage of the DUT to immediately collapse to the minimum voltage capability of the electronic load.

To test a CV/CC supply in both its CV and CC regions (an example - obtaining a V-I characteristic curve that spans both the CV and CC regions of operation), an electronic load set for constant resistance (CR) can be used. However, in an application such as an LLC converter where the control loop is strongly affected by the output impedance, use of a CR load will give results for loop compensation that are overly optimistic and will likely oscillate when tested with an actual low impedance battery load, especially at low input voltage/high battery voltage where the LLC converter is operating closest to resonance.

For final characterization and tuning the output control loops, a constant voltage load should be used.

Having said this, many electronic loads incorporate a constant voltage setting, but the output impedance of the load in this setting may not be sufficiently low (or too low) to successfully emulate a real-world battery impedance on. Simulating this impedance can be crucial in properly setting the compensation of the current control loop in order to prevent oscillation at low AC input voltage in a real-life application.

11.2 *Simulating Battery Characteristics with Electronic Load in CV Mode*

A Chroma 6314 mainframe with a 63106 load module was used to load the supply characterized in this report. The load impedance of the 63106 module in CV mode was measured using a bench supply and an HP3478A multimeter. The load module was configured in CV mode for 48 V, and the load voltage at the module input terminals was measured at currents of 1 A, 2 A, and 3 A. A ΔV of 1 mV was measured for a ΔI of 1 A into the load, indicating that the load module in CV mode has an impedance on the order of 1 m Ω . In reality, the load impedance may be lower, as the 1 m Ω measured may represent the resistance at the input terminals of the load module. This extremely low

impedance greatly exacerbates the tendency of the power supply output current to overshoot when started up into this load. Adding series resistance to approximate the actual battery characteristics helps control the overshoot and makes the testing conditions far more realistic.

The circuit described in this report is intended for charging a 42 V battery array consisting of 30 Sanyo/Panasonic UR16850RX Lithium ion cells (or equivalent), arranged as three parallel strings of 10 cells in series. The battery specification lists a cell impedance of 25 mΩ. Thus the impedance of the battery array is $(25 \times 10)/3$, or 83.3 mΩ. This impedance was approximated by using three paralleled 0.24 ohm, 2 W resistors in series with the electronic load used to test the supply. Below is a link to the battery data sheet:

<https://www.akkuparts24.de/mediafiles//Datenblaetter/Panasonic/Panasonic%20UR18650RX.pdf>

11.3 Efficiency

To make this measurement, the supply was powered with an AC source and loaded with an electronic load in CR mode. The maximum load was adjusted to be just short of the current limit of the UUT. The figure shown includes the efficiency of the LLC stage combined with that of the standby/bias flyback supply.

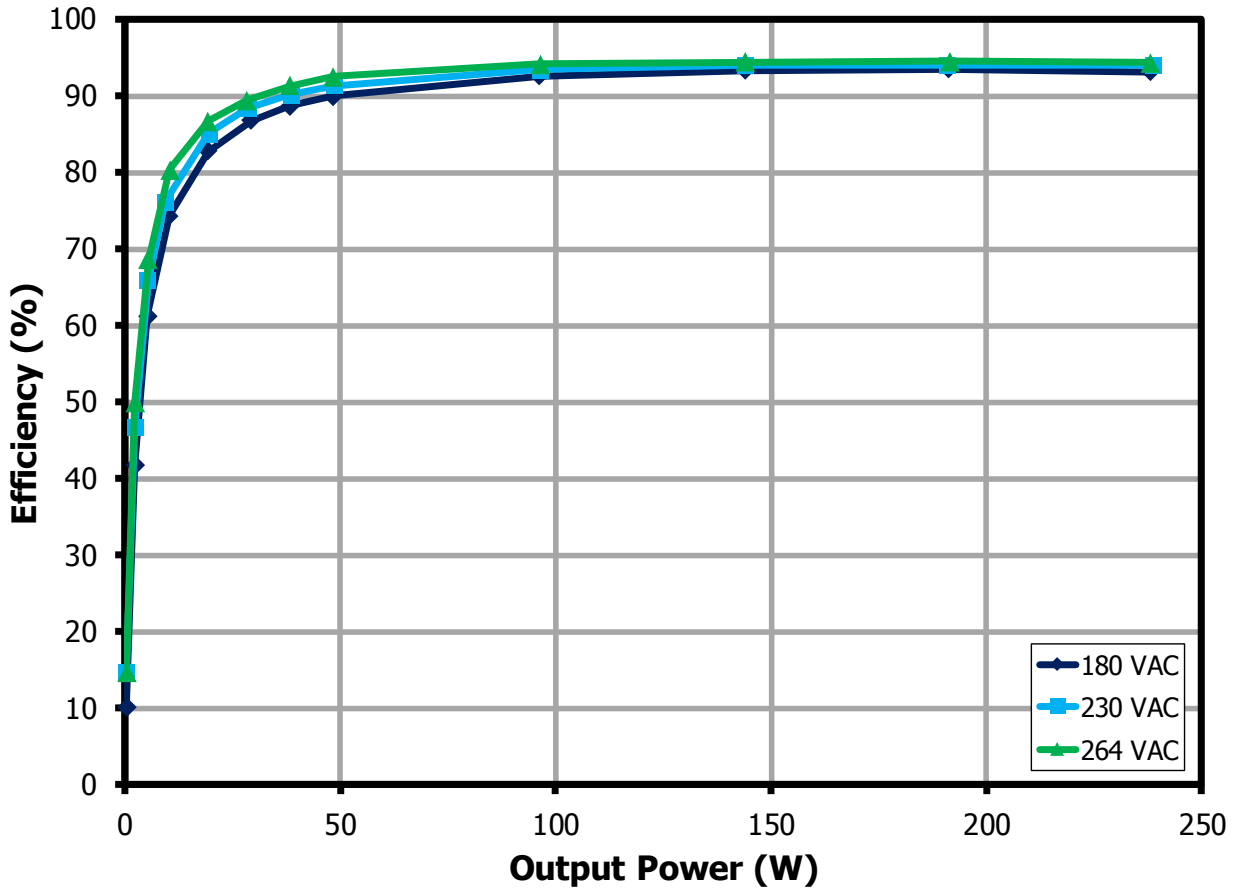


Figure 20 – Efficiency vs. Load, AC Input.



11.4 *V-I Characteristic, Constant Resistance Load*

The V-I characteristic showing the transition from constant voltage mode to constant current mode was measured using an electronic load set for constant resistance to allow proper operation of the DUT in both CV and CC mode. The measurements cut off at 20 V, which is lower than the recommended discharge voltage of the intended battery array (24 V).

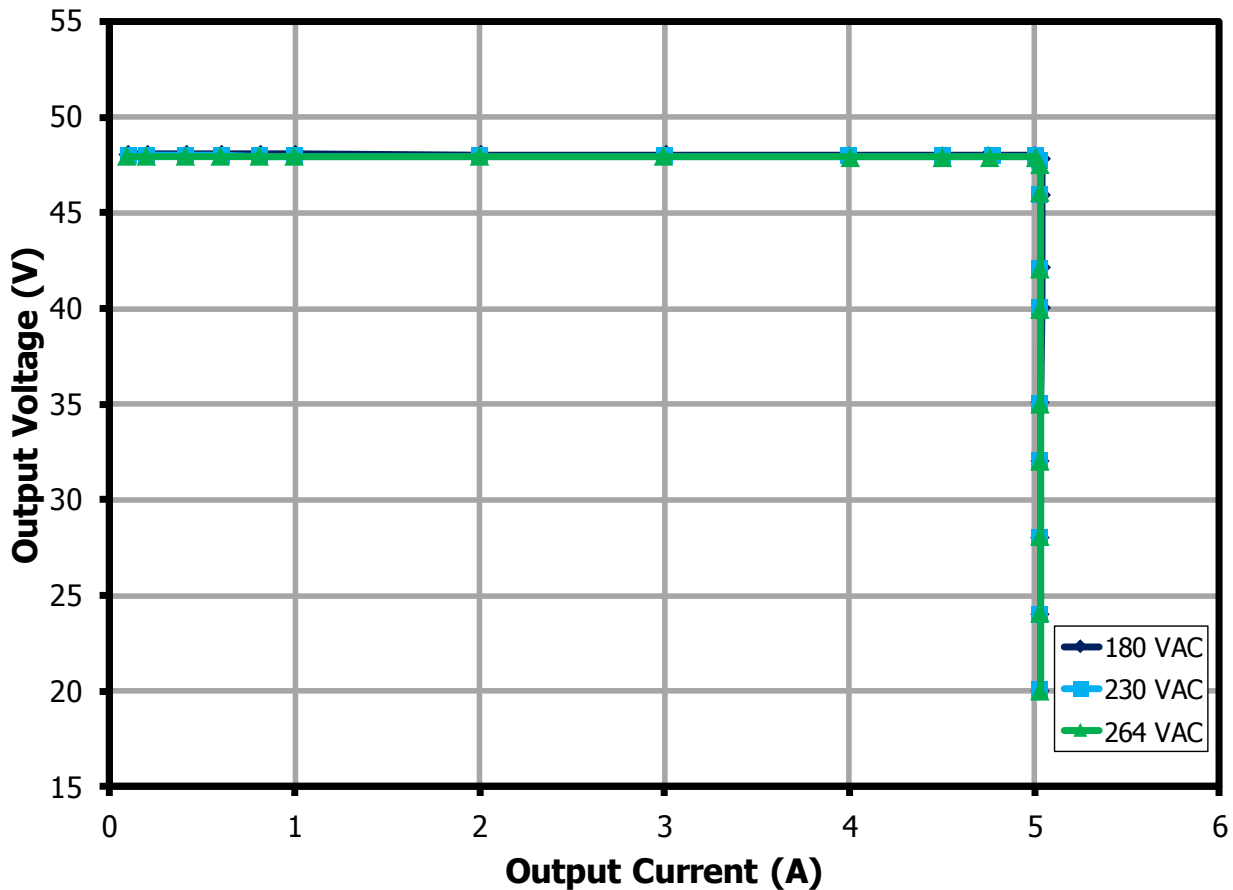


Figure 21 – V-I Characteristic with CR Load.

11.5 **Output V-I Characteristic, Constant Voltage Load**

The V-I characteristic in constant current mode was measured using a Chroma 63106 electronic load module set for constant voltage, with 80 mΩ in series to simulate battery impedance. The output current was measured using a Fluke 87 DVM, as the current readings were not steady on the electronic load. Voltage was measured using a Fluke 77 IV DVM connected directly at the supply output. The slight kink in output current shown in Figure 22 is due to a small drift in output current limit during extended testing.

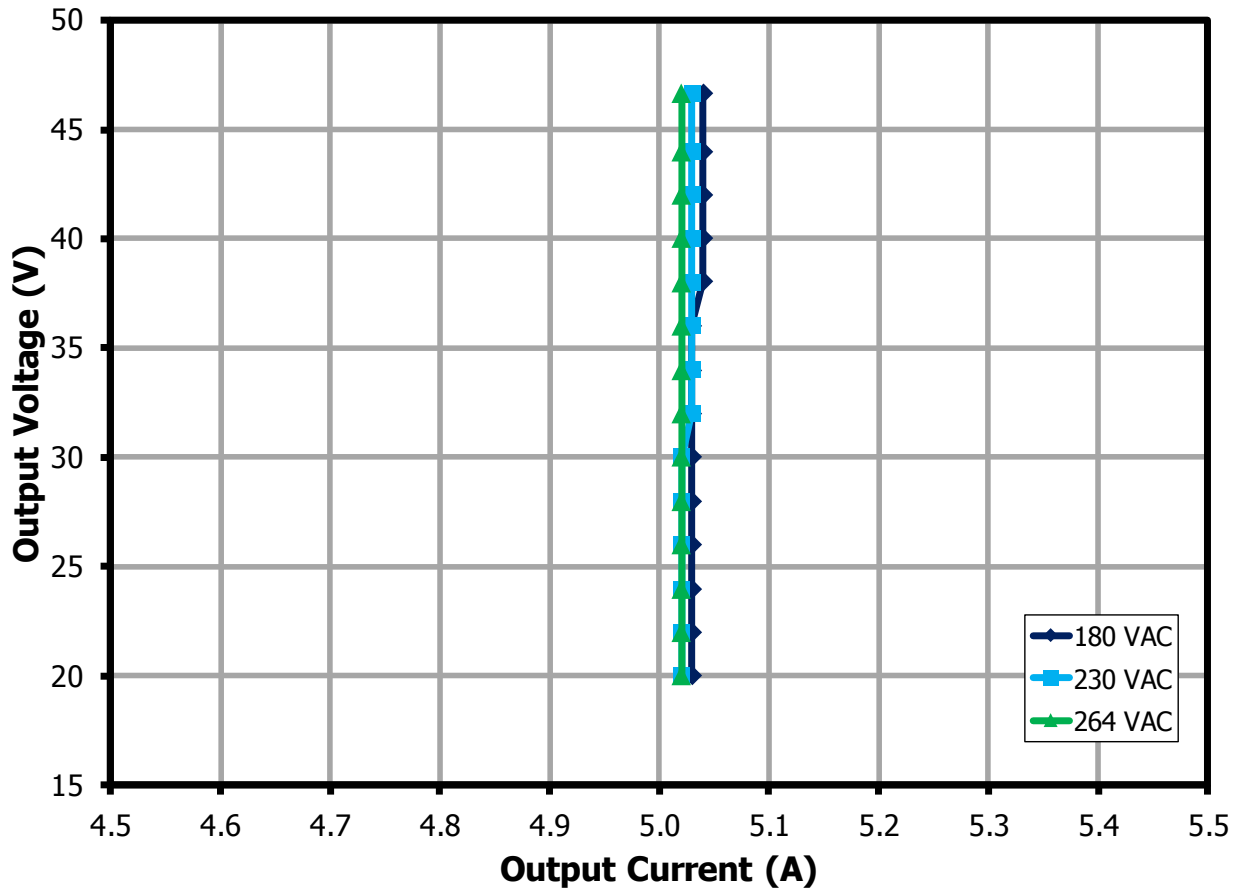


Figure 22 – V-I Characteristic with CV Load.

11.6 **Operating Frequency vs. Output Voltage Characteristic**

To obtain the data for Figure 23, the supply was loaded with a Chroma 63106 load module operating in CV mode, with an 80 mΩ resistor inserted in series to simulate battery impedance. Operating frequency was measured using a LeCroy 64Xi oscilloscope. Since the operating frequency is modulated by the supply B+ ripple voltage, the statistics function of the oscilloscope was used to obtain the mean operating frequency, shown in the figure below. Output voltage was measured using a Fluke 77 IV DVM connected directly at the supply output. There is considerable fluctuation of the operating frequency around the mean value due to B+ ripple, especially at low line.

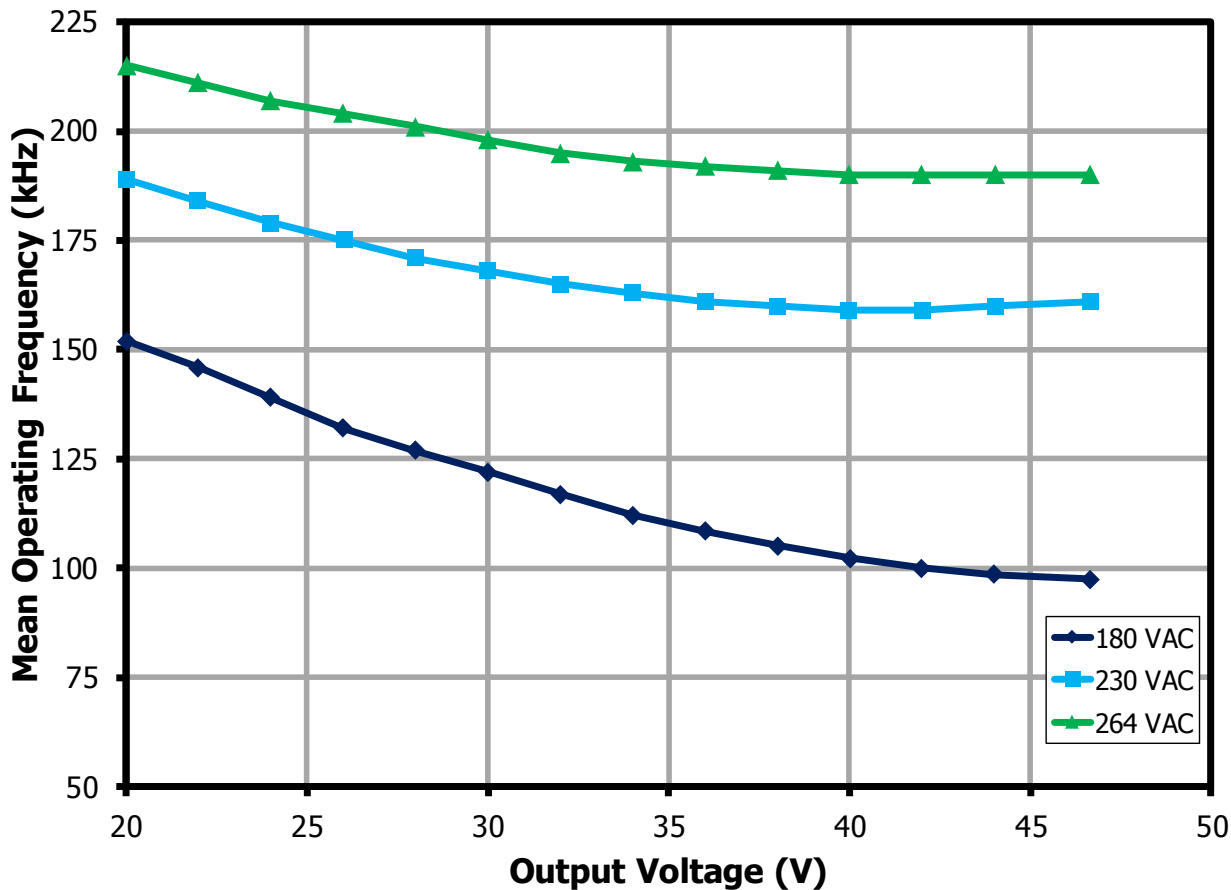


Figure 23 – $f_{MEAN}-V_{OUT}$ Characteristic with CV load.

12 Waveforms

12.1 LLC Primary Voltage and Current

The LLC stage primary current was measured by inserting a current sensing loop in series with the ground side of resonating capacitor C14. The power supply output was loaded with an electronic load set for a constant voltage characteristic, with an 80 mΩ resistor in series to simulate battery impedance. Waveforms were gathered for load settings yielding output voltages of 40 V (just after current limit), 32 V, and 24 V (the lower operating limit of the battery array).

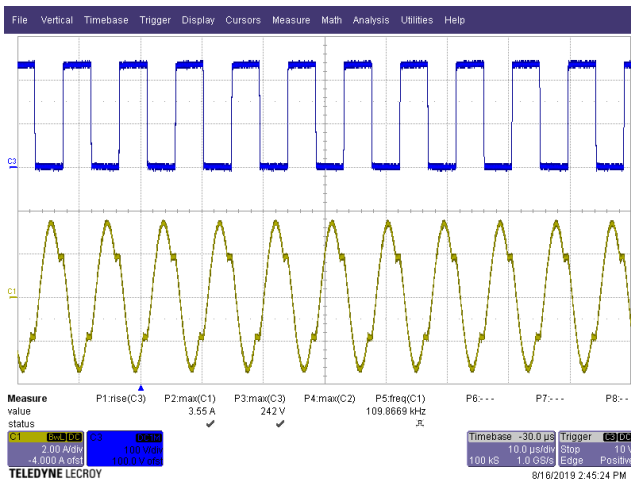


Figure 24 – LLC Stage Primary Voltage and Current, 180 VAC Input, CR Load, 40 V Load Setting.

Upper: Current, 2 A / div.

Lower: Voltage, 100 V, 5 μs / div.

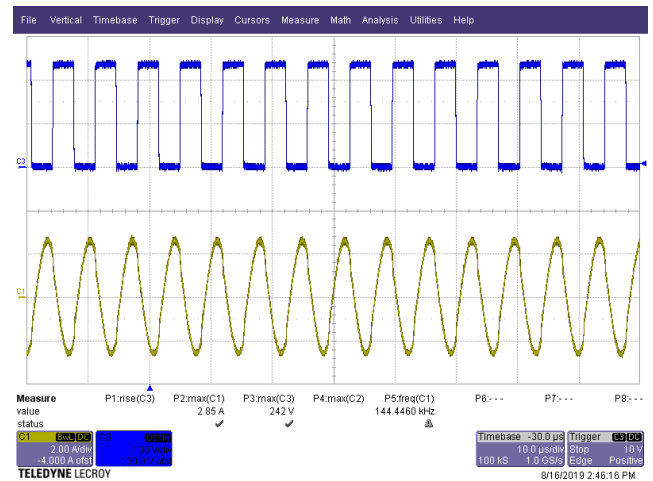


Figure 25 – LLC Stage Primary Voltage and Current, 180 VAC Input, CR Load, 24 V Load Setting.

Upper: Current, 2 A / div.

Lower: Voltage, 100 V, 5 μs / div.

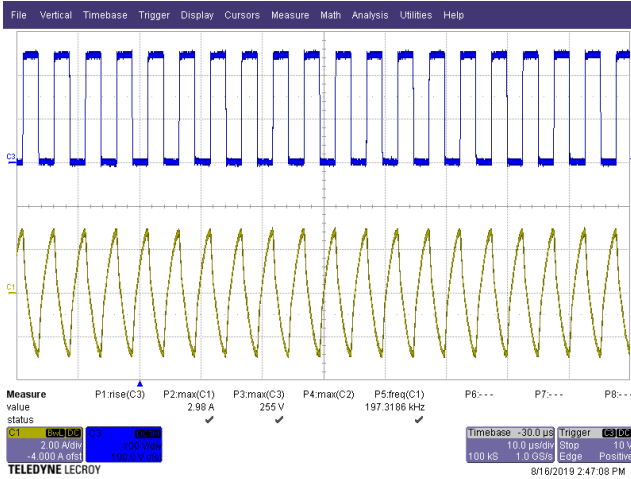


Figure 26 – LLC Stage Primary Voltage and Current, 180 VAC Input, CR Load, 12 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

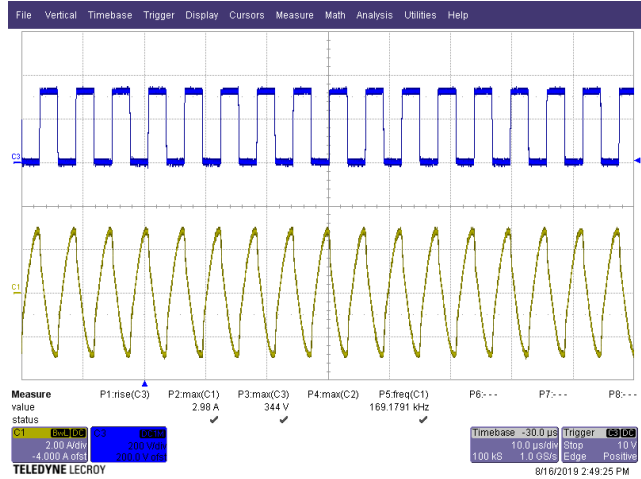


Figure 27 – LLC Stage Primary Voltage and Current, 230 VAC Input, CR Load, 40 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

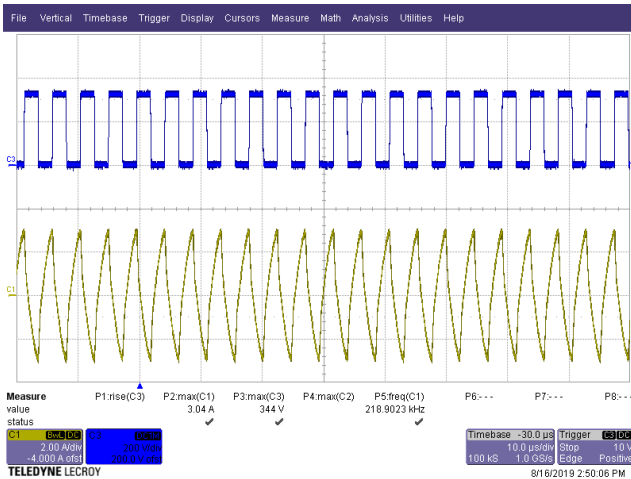


Figure 28 – LLC Stage Primary Voltage and Current, 230 VAC Input, CR Load, 32 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

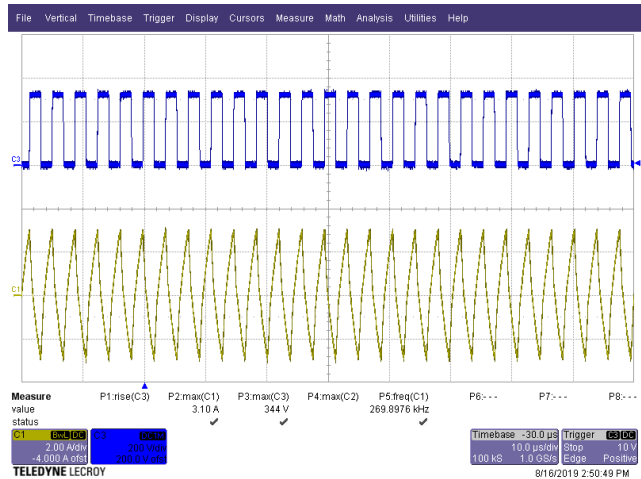


Figure 29 – LLC Stage Primary Voltage and Current, 230 VAC Input, CR Load, 24 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

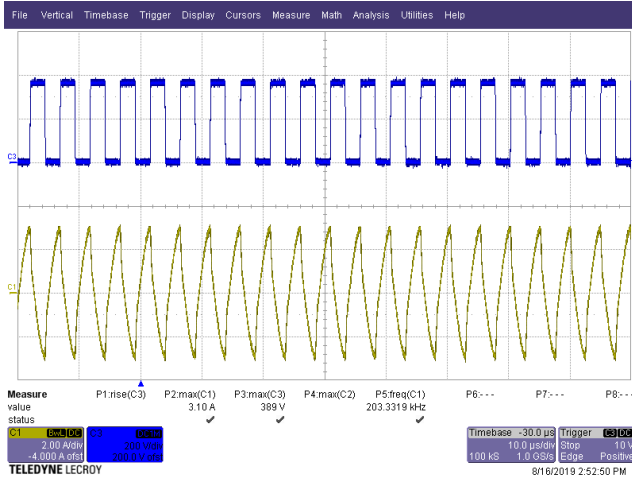


Figure 30 – LLC Stage Primary Voltage and Current, 264 VAC Input, CR Load, 48 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

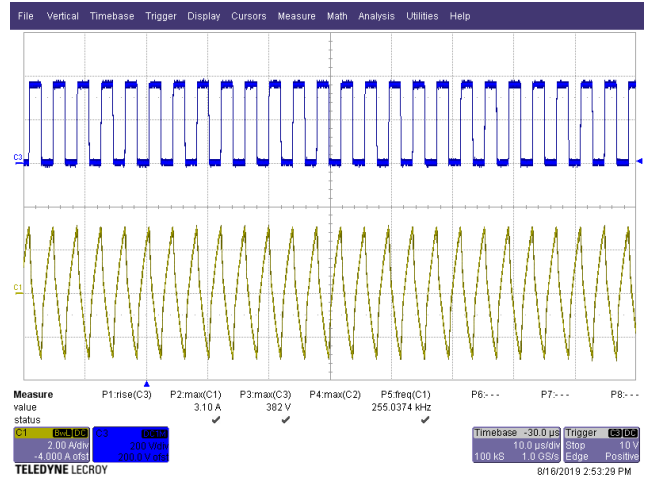


Figure 31 – LLC Stage Primary Voltage and Current, 264 VAC Input, CR Load, 24 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

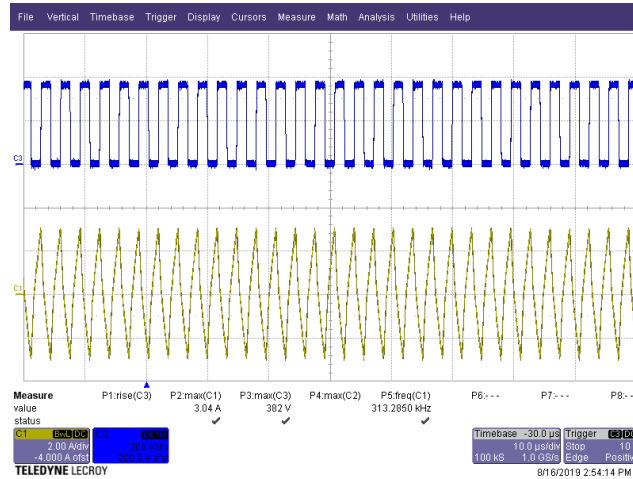


Figure 32 – LLC Stage Primary Voltage and Current, 264 VAC Input, CR Load, 12 V Load Setting.
Upper: Current, 2 A / div.
Lower: Voltage, 100 V, 5 μ s / div.

12.2 Output Rectifier Peak Reverse Voltage

Since a full-wave bridge is used at the output of this supply, output diode PIV requirements are relaxed, and 60 V Schottky diodes can be used.

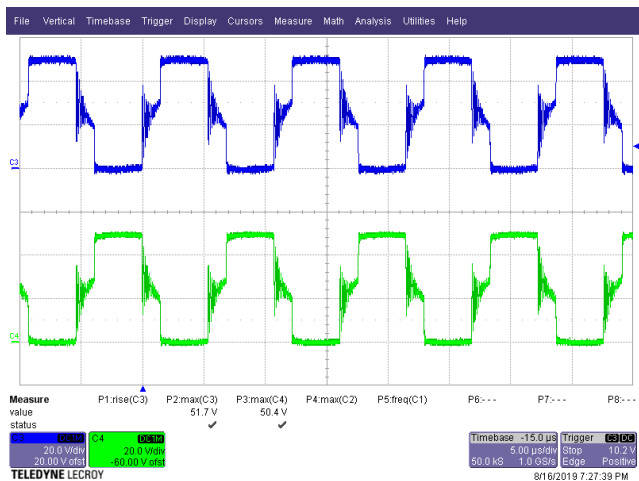


Figure 33 – Output Rectifier (D4 & D5) Reverse Voltage, 180 VAC, 47 V, 5 A Load.
 Blue: Input 1 PIV, 20 V / div.
 Green: Input 2 PIV, 20 V, 2 μs / div.
 Rectifier PIV at 230 VAC is 83% of Maximum Rating for 60 V Schottky Diode.

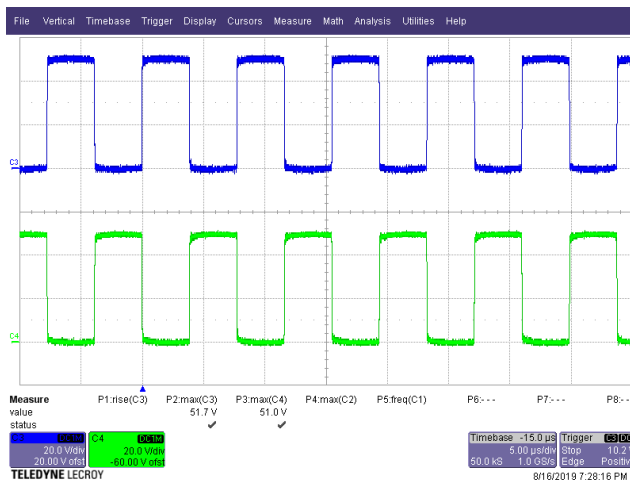


Figure 34 – Output Rectifier (D4 & D5) Reverse Voltage, 230 VAC, 47 V, 5 A Load.
 Blue: D4 PIV, 20 V / div.
 Green: D5 PIV, 20 V, 2 μs / div.
 Rectifier PIV at 230 VAC is 83% of Maximum Rating for 60 V Schottky Diode.

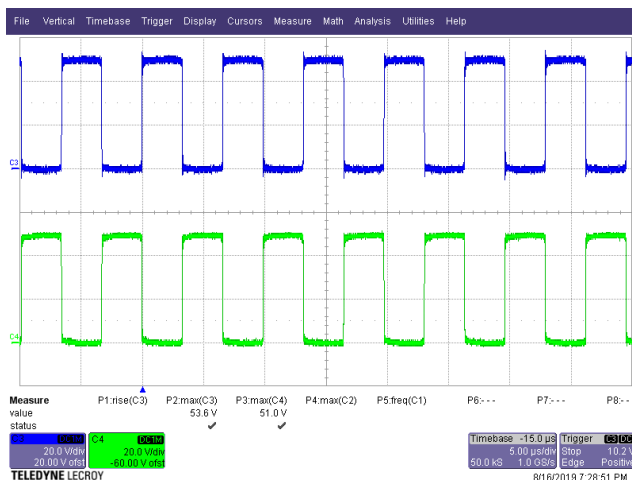


Figure 35 – Output Rectifier (D4 & D5) Reverse Voltage, 264 VAC, 47 V, 5 A Load.
 Upper: D4 PIV, 20 V / div.
 Lower: D5 PIV, 20 V, 2 μs / div.
 Rectifier PIV at 264 VAC is 83% of Maximum Rating for 60 V Schottky Diode.

12.3 **LLC Start-up Output Voltage and Current, Transformer Primary Current Using Constant Voltage Output Load**

This series of figures shows the peak output and transformer T1 primary current during startup into a CV load. An 80 mΩ resistor is placed in series with the CV load to simulate the impedance of a 10 deep by 3 wide array of Lithium ion cells similar to the Sanyo/PanasonicUR18650RX. Adding the additional impedance reduces the overshoot current at startup. Due to the wide range of input and output voltages for an LLC supply operating as a battery charger with rectified mains input, it is not possible to adjust the current sense amplifier compensation for maximum bandwidth to substantially suppress output current overshoot when starting into a CV load and simultaneously ensure stability under all operating conditions. The primary overcurrent limit should be adjusted with sufficient operating margin to allow startup without triggering overcurrent protection.

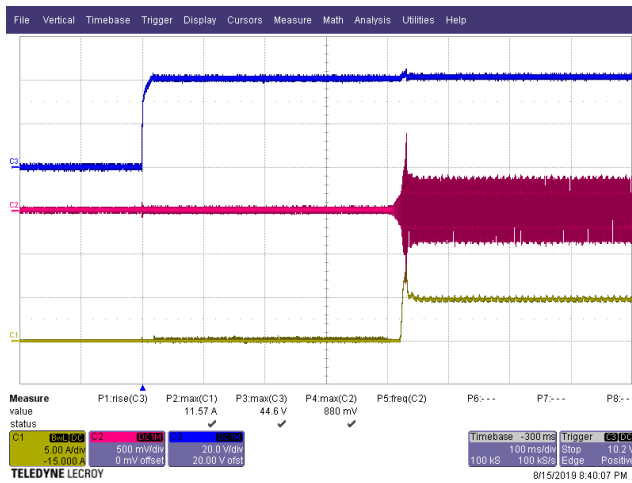


Figure 36 – 180 VAC Start-up, 40 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

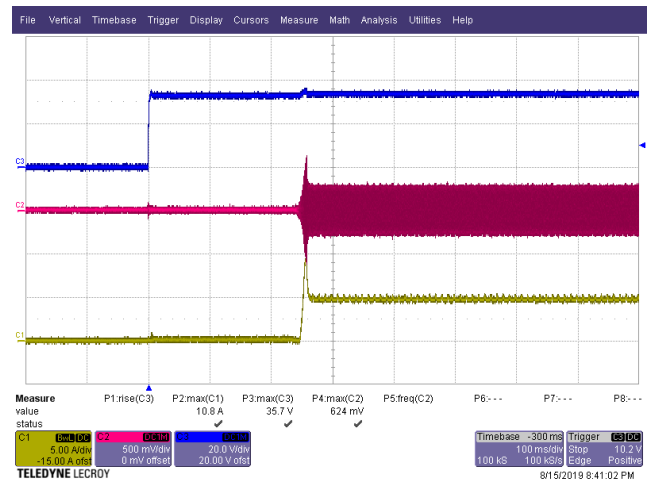


Figure 37 – 180 VAC Start-up, 32 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

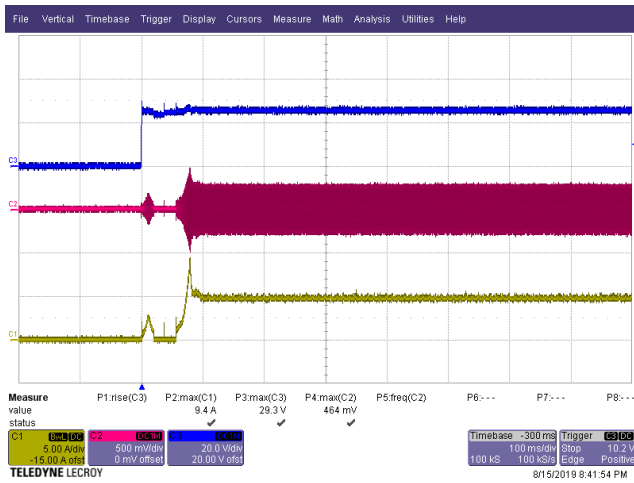


Figure 38 – 180 VAC Start-up, 24 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

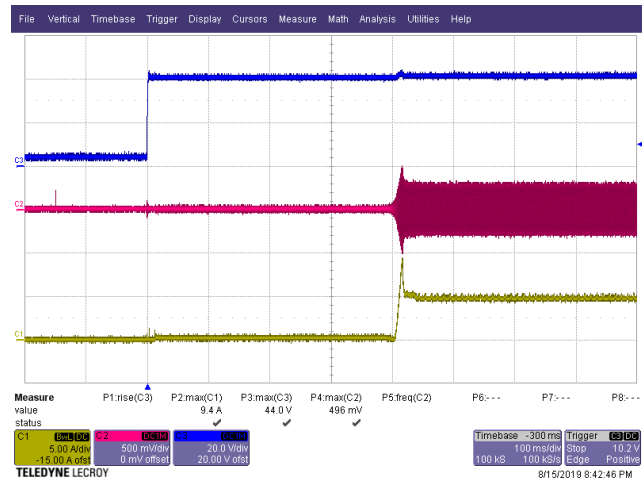


Figure 39 – 230 VAC Start-up, 40 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

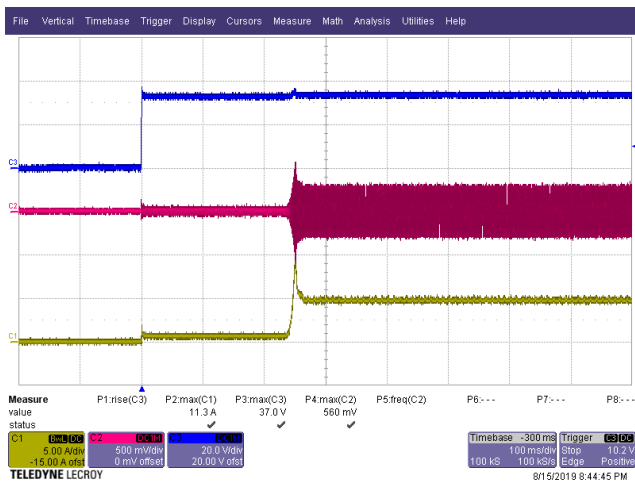


Figure 40 – 230 VAC Start-up, 32 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

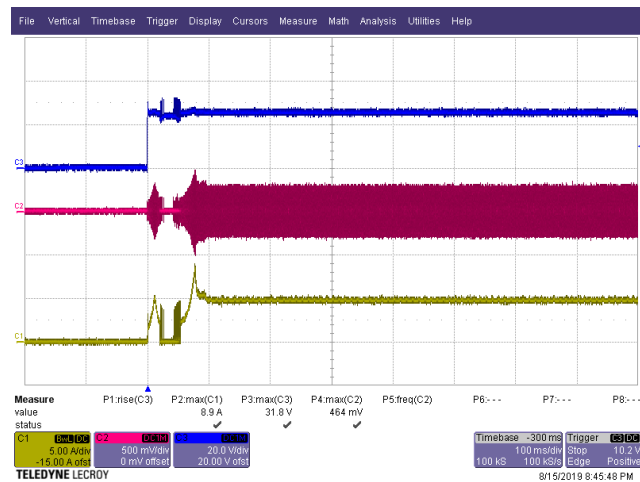


Figure 41 – 230 VAC Start-up, 24 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT} , 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT} , 5 A, 100 ms / div.

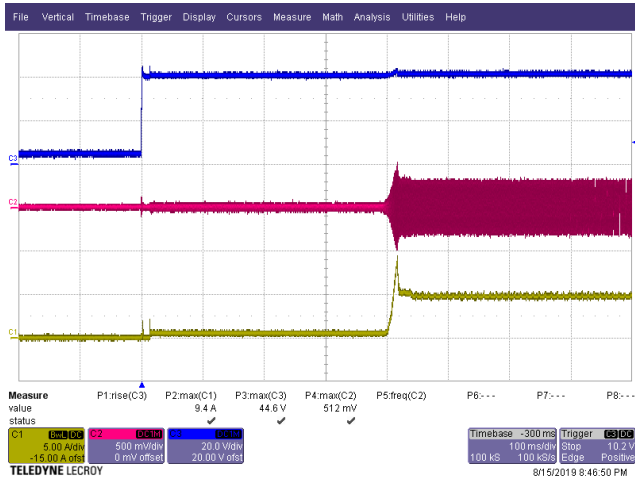


Figure 42 – 264 VAC Start-up, 40 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT}, 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT}, 5 A, 100 ms / div.

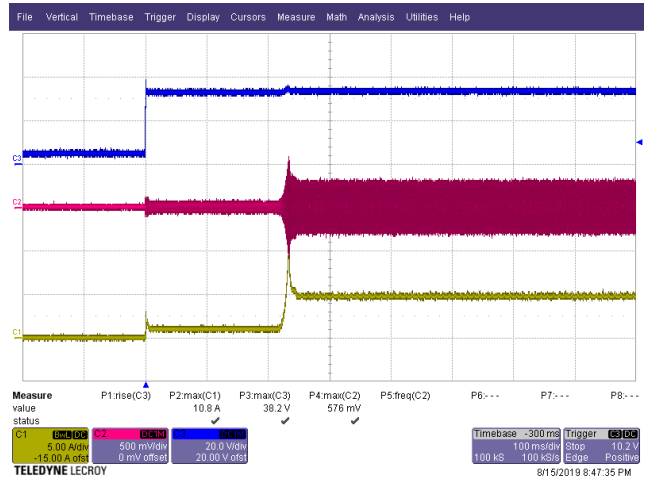


Figure 43 – 264 VAC Start-up, 32 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT}, 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT}, 5 A, 100 ms / div.

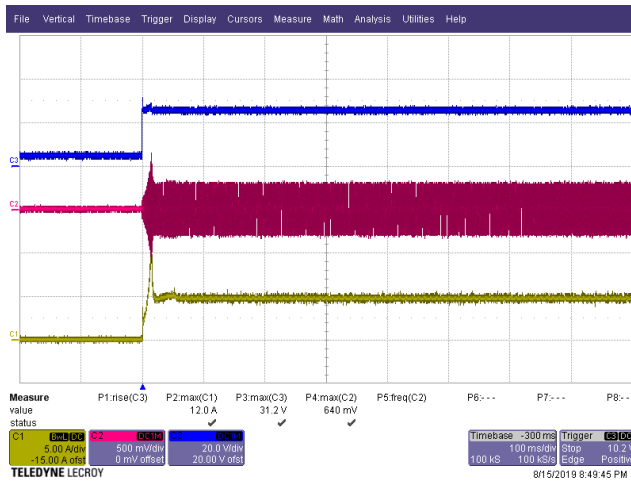


Figure 44 – 264 VAC Start-up, 24 V CV Load with 80 mΩ Series Resistor.
 Blue – V_{OUT}, 20 V / div.
 Red – Primary Current, 500 mV / 5 A / div.
 Yellow – I_{OUT}, 5 A, 100 ms / div.

12.4 *Output Ripple Measurements*

12.4.1 *Ripple Measurement Technique*

For DC output ripple measurements a modified oscilloscope test probe is used to reduce spurious signals. Details of the probe modification are provided in the figures below.

Tie two capacitors in parallel across the probe tip of the 4987BA probe adapter. Use a 0.1 μF / 50 V ceramic capacitor and 1.0 μF / 100 V aluminum electrolytic capacitor. The aluminum-electrolytic capacitor is polarized, so always maintain proper polarity across DC outputs.

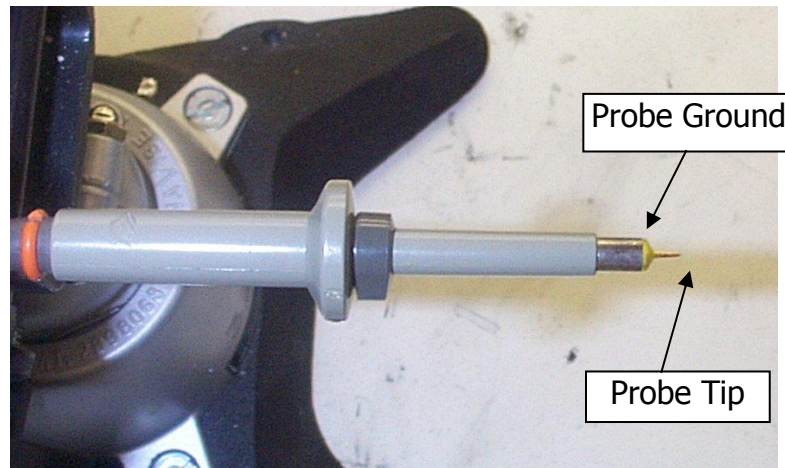


Figure 45 – Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

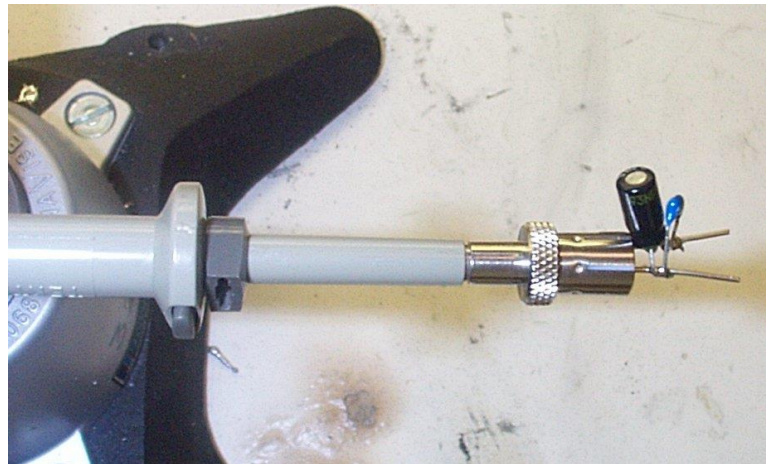


Figure 46 – Oscilloscope Probe with Probe Master 4987BA BNC Adapter (Modified with Wires for Probe Ground for Ripple measurement and Two Parallel Decoupling Capacitors Added).

12.4.2 *Ripple Measurements*

These measurements were taken using a Chroma 63106 electronic load module set in CV mode, with 80 mΩ inserted in series to simulate the battery impedance. Output ripple voltage and current ripple measurements were made using AC coupled probes.

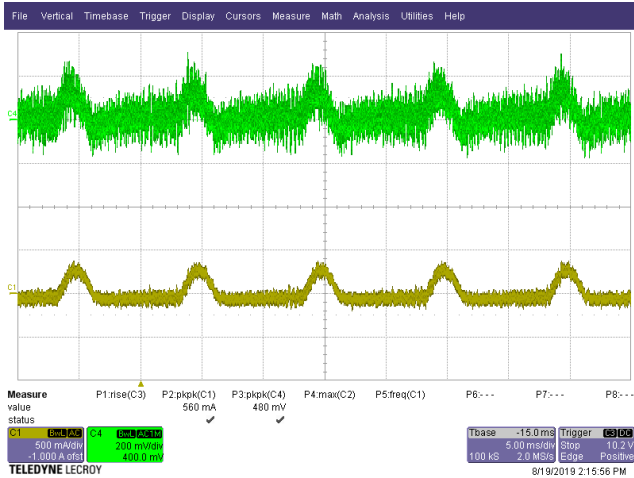


Figure 47 – Output Ripple, 180 VAC, 40 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.



Figure 48 – Output Ripple, 180 VAC, 40 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

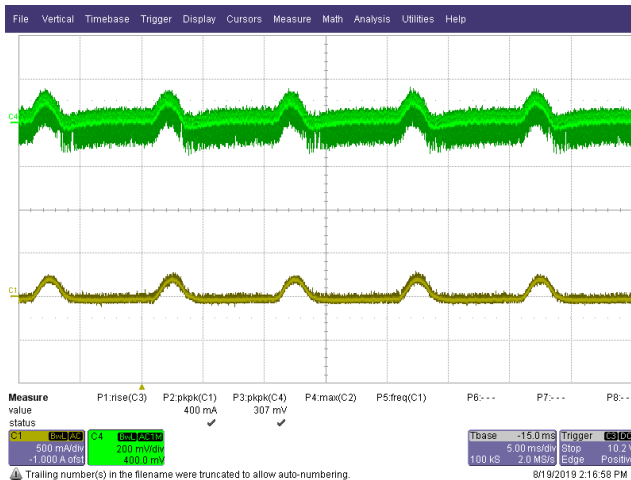


Figure 49 – Output Ripple, 180 VAC, 24 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

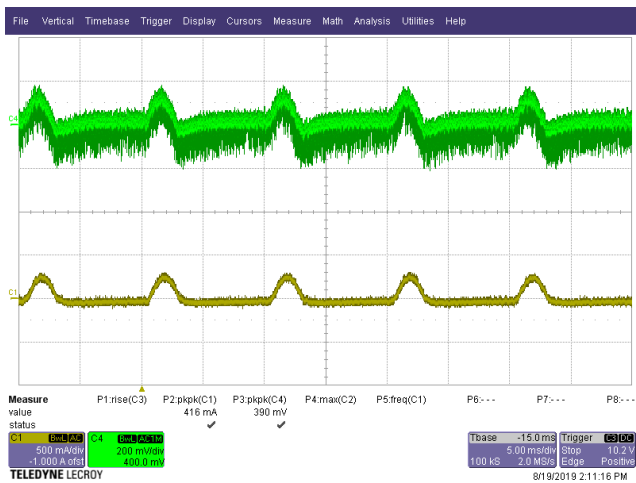


Figure 50 – Output Ripple, 230 VAC, 40 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

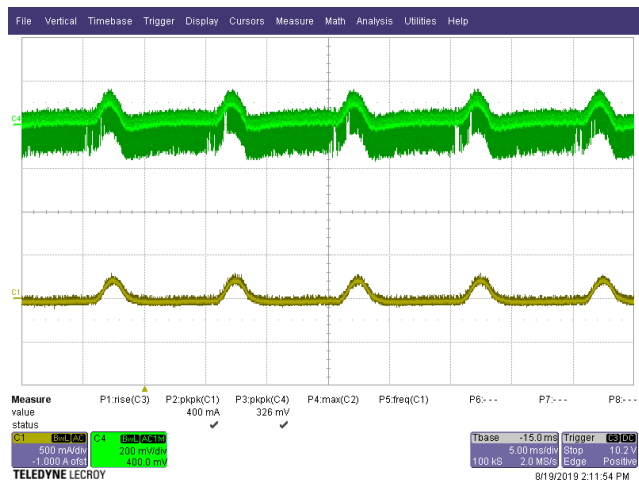


Figure 51 – Output Ripple, 230 VAC, 32 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

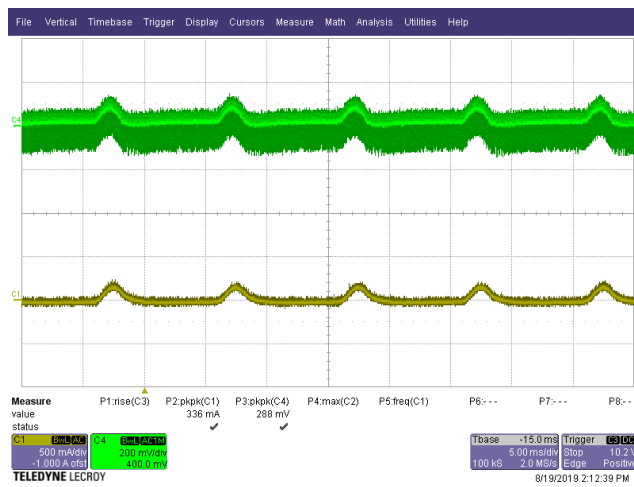


Figure 52 – Output Ripple, 230 VAC, 24 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

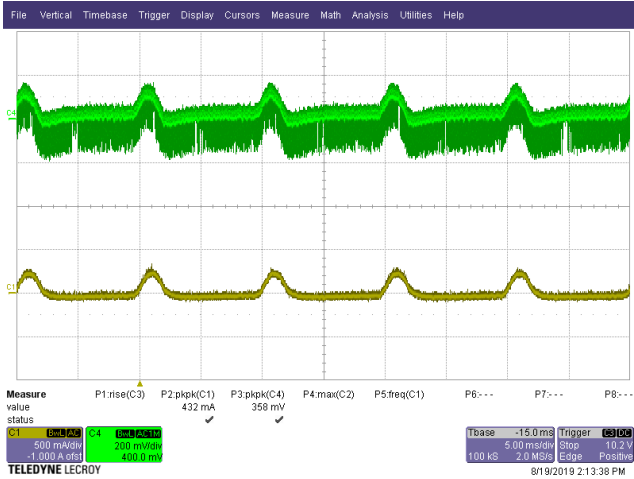


Figure 53 – Output Ripple, 264 VAC, 40 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.



Figure 54 – Output Ripple, 264 VAC, 32 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.

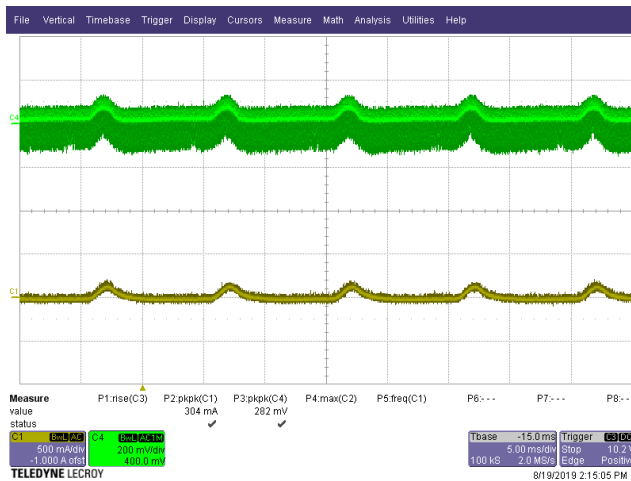


Figure 55 – Output Ripple, 264 VAC, 24 V CV Load.
 Green: V_{OUT} Ripple, 200 mV / div.
 Yellow: I_{OUT} Ripple, 500 mA, 5 ms / div.



13 Temperature Profiles

The board was operated at room temperature, with output set at maximum using a constant voltage load. For each test condition the unit was allowed to thermally stabilize (~ 1 hr) before measurements were made.

13.1 Spot Temperature Measurements

Position	Temperature ($^{\circ}\text{C}$)		
	180 VAC	230 VAC	264 VAC
T1	82.3 (wdg) / 70 (core)	83.3 (wdg) / 70.8 (core)	82.8 (wdg) / 68.7 (core)
BR1	66.9	58.6	54.1
U1	79.4	68.7	62.3
D12	81.6	81	79.5
D14	75.4	72.8	71.8
D13	79.5	76.4	75.4
AMB	24	24	24

13.2 180 VAC, 60 Hz, 100% Load Temperature Profile

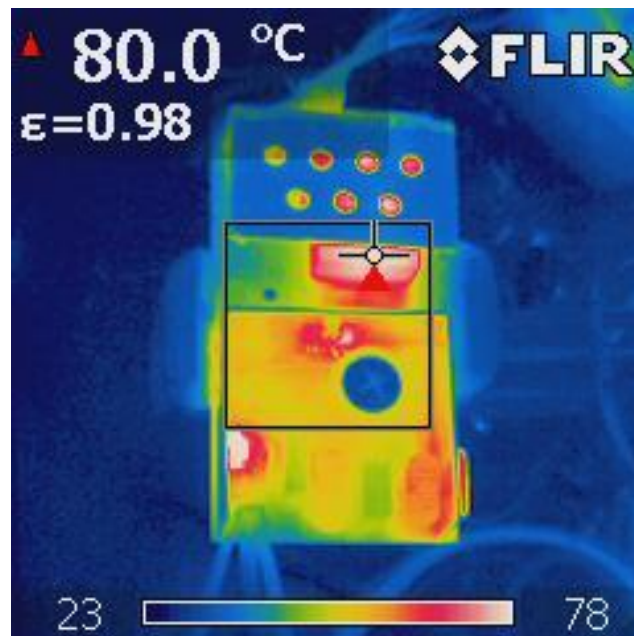


Figure 56 – Top View Thermal Picture, 180 VAC.

13.3 **230 VAC, 60 Hz, 100% Load Temperature Profile**

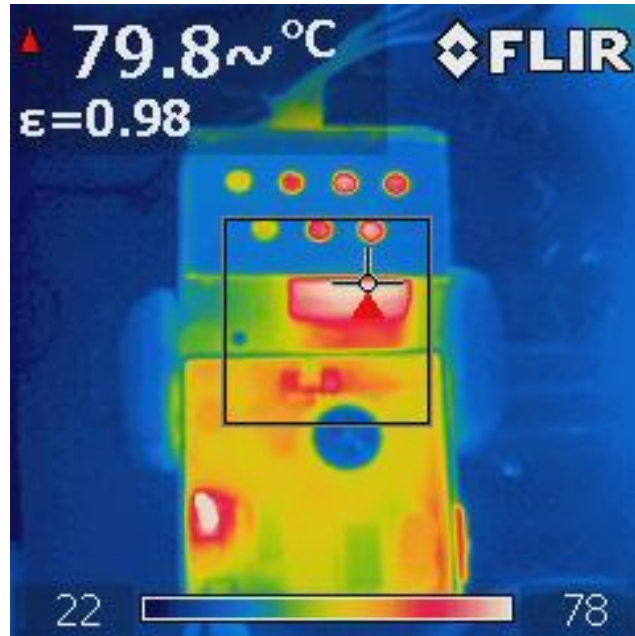


Figure 57 – Top View Thermal Picture, 100% Load, 230 VAC.

13.4 **264 VAC, 60 Hz, 100% Load Temperature Profile**

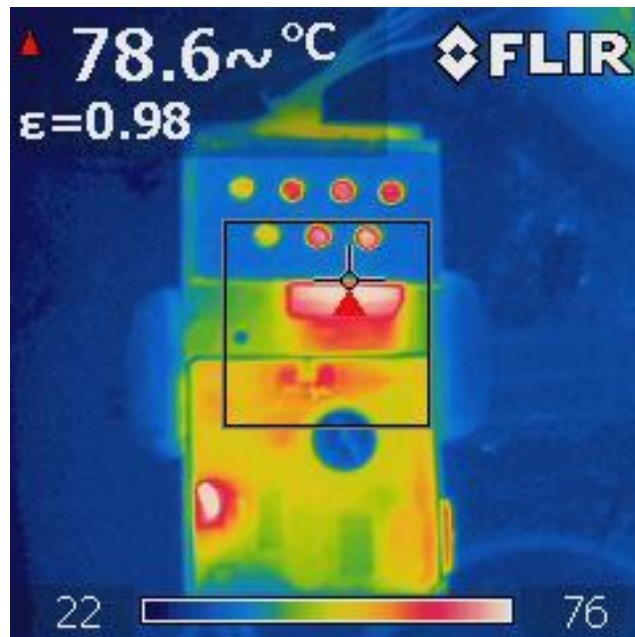


Figure 58 – Top View Thermal Picture, 100% Load, 264 VAC.

14 Constant Voltage Output Gain-Phase

Constant voltage output gain-phase was tested using a Chroma 63106 electronic load module in constant current mode, at output loads of 2 A and 4 A.

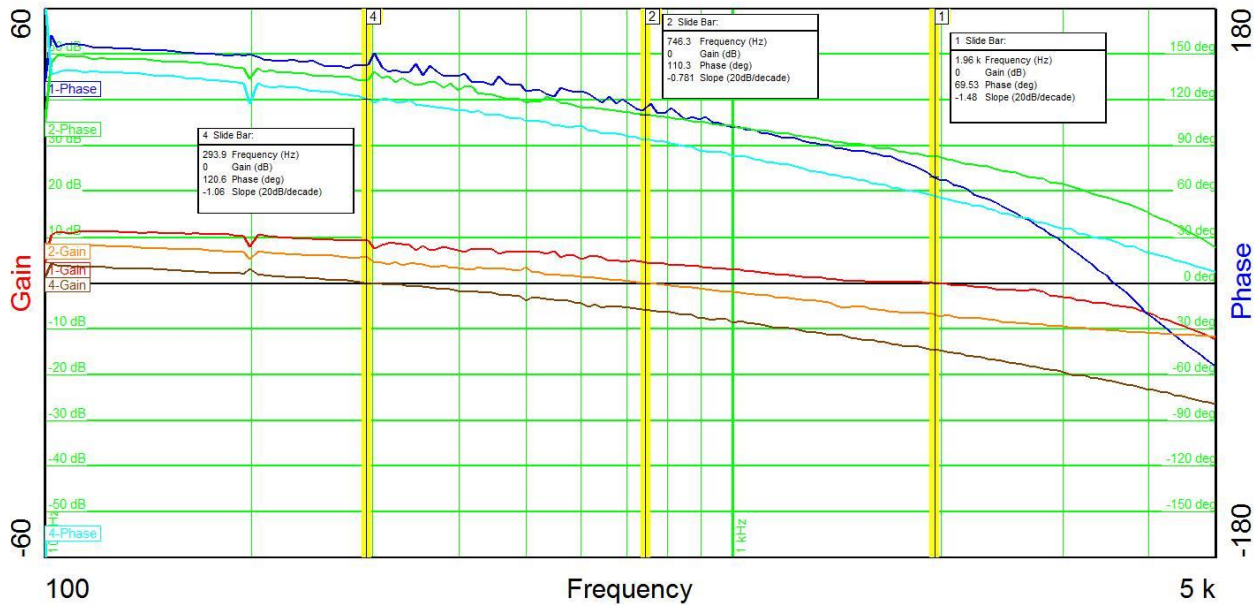


Figure 59 – Constant Voltage Output Gain-Phase, 2 A CC Load.
 Red/Blue – 180 VAC Gain-Phase, Crossover Frequency 1.96 kHz, Phase Margin 69.5°.
 Orn/Grn – 230 VAC Gain-Phase, Crossover Frequency 746 Hz, Phase Margin 110°.
 Brn/Aqua – 264 VAC Gain-Phase, Crossover Frequency 294 Hz, Phase Margin 121°.



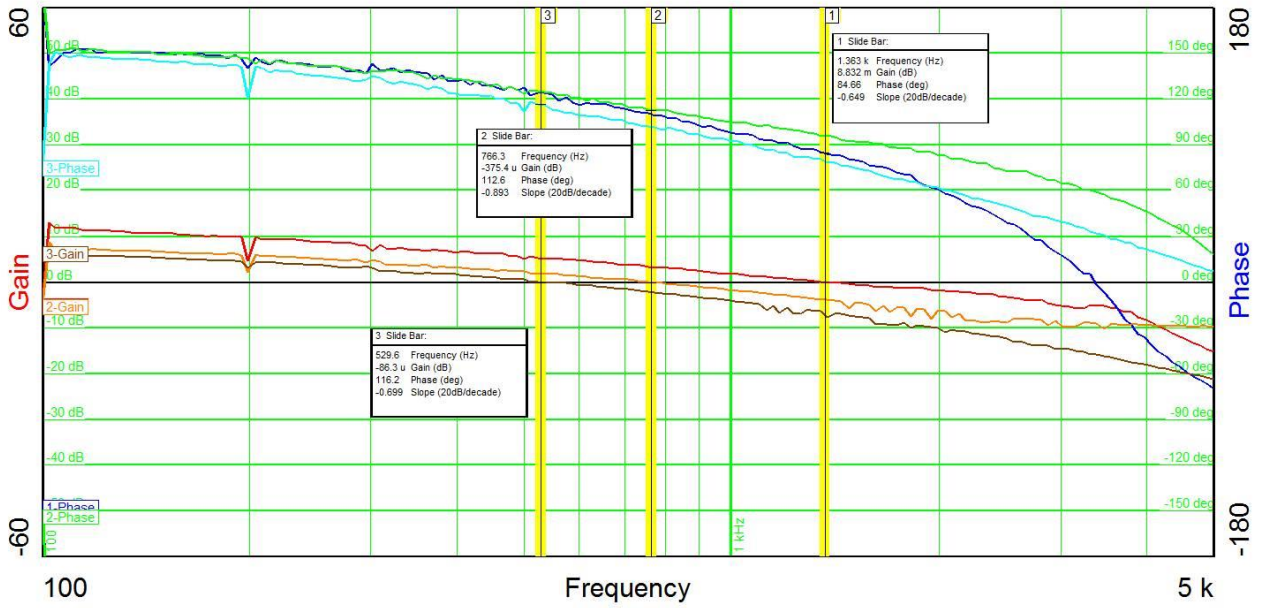


Figure 60 – Constant Voltage Output Gain-Phase, 4 A CC Load.
 Red/Blue – 180 VAC Gain-Phase, Crossover Frequency 1.36 kHz, Phase Margin 65°.
 Orn/Grn – 230 VAC Gain-Phase, Crossover Frequency 766 Hz, Phase Margin 113°.
 Brn/Aqua – 264 VAC Gain-Phase, Crossover Frequency 530 Hz, Phase Margin 116°.



15 Constant Current Output Gain-Phase

Current mode gain-phase was tested using a Chroma 63106 electronic load module set to constant voltage mode, with an 80 mΩ series resistance inserted in series with the output cable to better approximate the impedance of a 10 deep X 3 wide array (42 V nominal) of Sanyo UR18650RX (or equivalent) Lithium cells. Load settings were 40V, 32V, and 24V to examine the gain and phase at different points of the battery charge curve. Testing was also done at input voltages of 180 VAC, 230 VAC, and 264 VAC, as the input voltage also affects the supply characteristics when a PFC is not used at the input to provide a regulated B+ for the LLC DC-DC converter stage.

Using a CV load maximizes the CC loop gain (worst case for control loop) and simulates operating while charging a battery. Using the constant resistance setting for the electronic load will yield overly optimistic results for gain-phase measurements and for determining component values for frequency compensation.

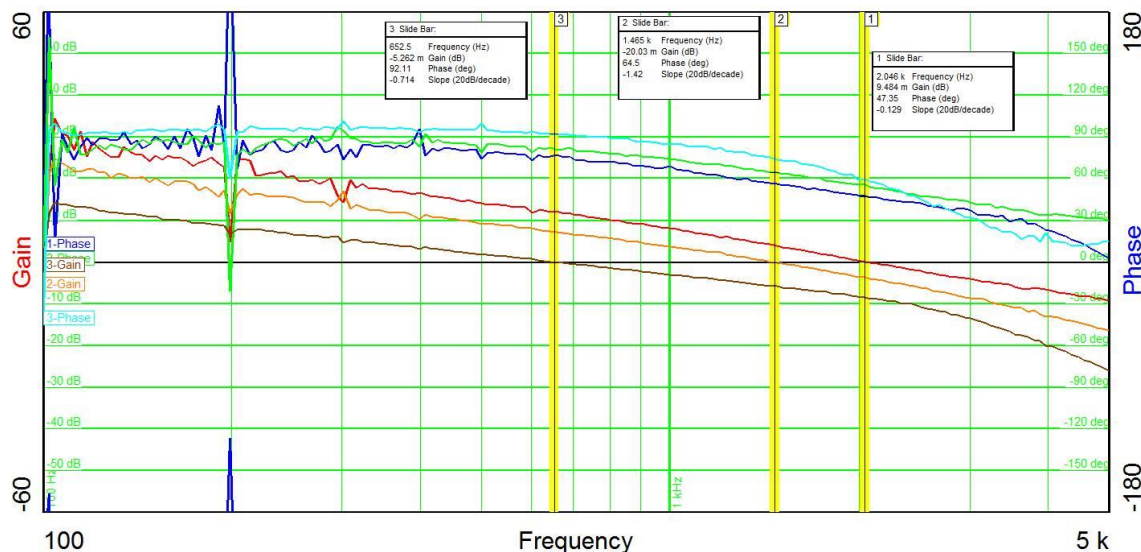


Figure 61 – LLC Converter Gain-Phase, Constant Current Output, 180 VAC Input, Constant Voltage Load with 80 mΩ Series Resistance.

- Red/Blue – 40 Vo Gain and Phase - Crossover Frequency – 2 kHz, Phase Margin – 47°.
- Orange/Green – 32 Vo Gain and Phase - Crossover Frequency – 1.46 kHz, Phase Margin – 64°.
- Brown/Aqua – 24 Vo Gain and Phase - Crossover Frequency – 652 Hz, Phase Margin – 92°.

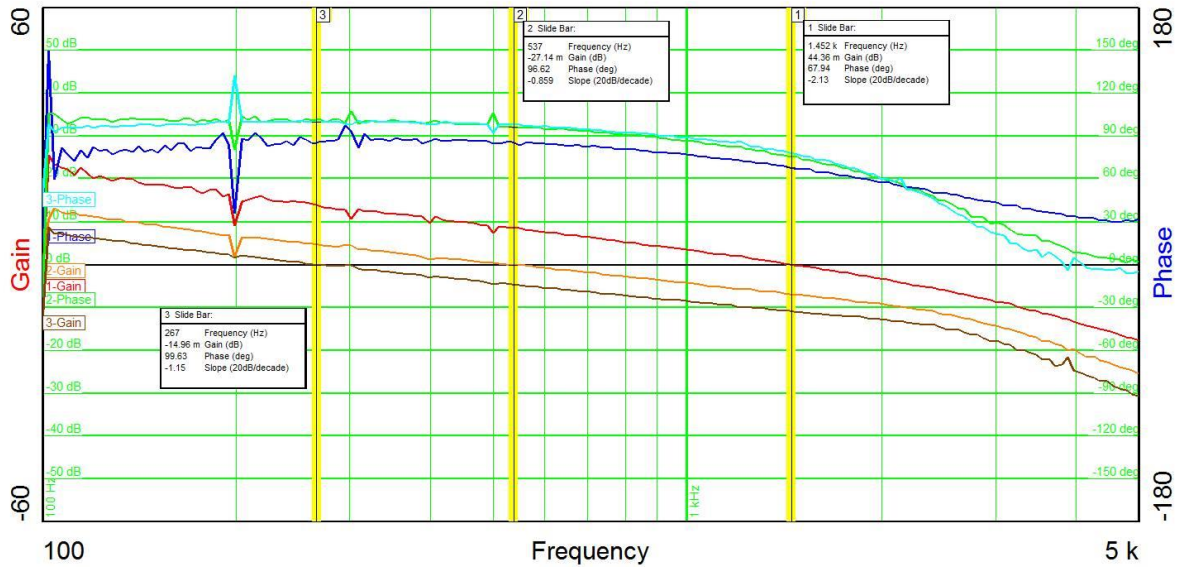


Figure 62 – LLC Converter Gain-Phase, Constant Current Output, 230 VAC Input, Constant Voltage Load with 80 mΩ Series Resistance.

Red/Blue – 40Vo Gain and Phase, Crossover Frequency – 1.45 kHz, Phase Margin – 68°.
 Orange/Green – 32 Vo VAC Gain and Phase Crossover Frequency – 537 Hz, Phase Margin – 97°.
 Brown/Aqua – 24 Vo VAC Gain and Phase Crossover Frequency – 267 Hz, Phase Margin – 100°.

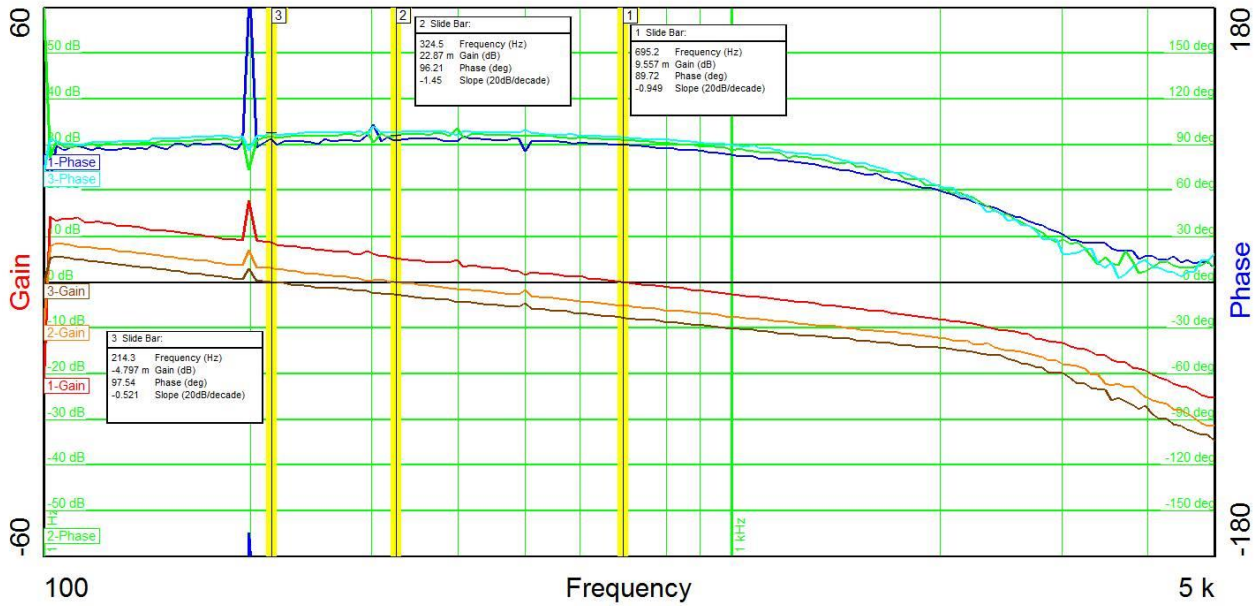


Figure 63 – LLC Converter Gain-Phase, Constant Current Output, 264 VAC Input, Constant Voltage Load with 80 mΩ Series Resistance.

Red/Blue – 40 Vo Gain and Phase, Crossover Frequency – 695 kHz, Phase Margin – 90°.
 Orange/Green – 32 Vo VAC Gain and Phase Crossover Frequency – 324 Hz, Phase Margin – 96°.
 Brown/Aqua – 24 Vo VAC Gain and Phase Crossover Frequency – 214 Hz, Phase Margin – 97°.

16 Conducted EMI

Conducted EMI tests were performed using a floating resistive load (9 Ω).



Figure 64 – EMI Set-up with Floating Resistive Load.

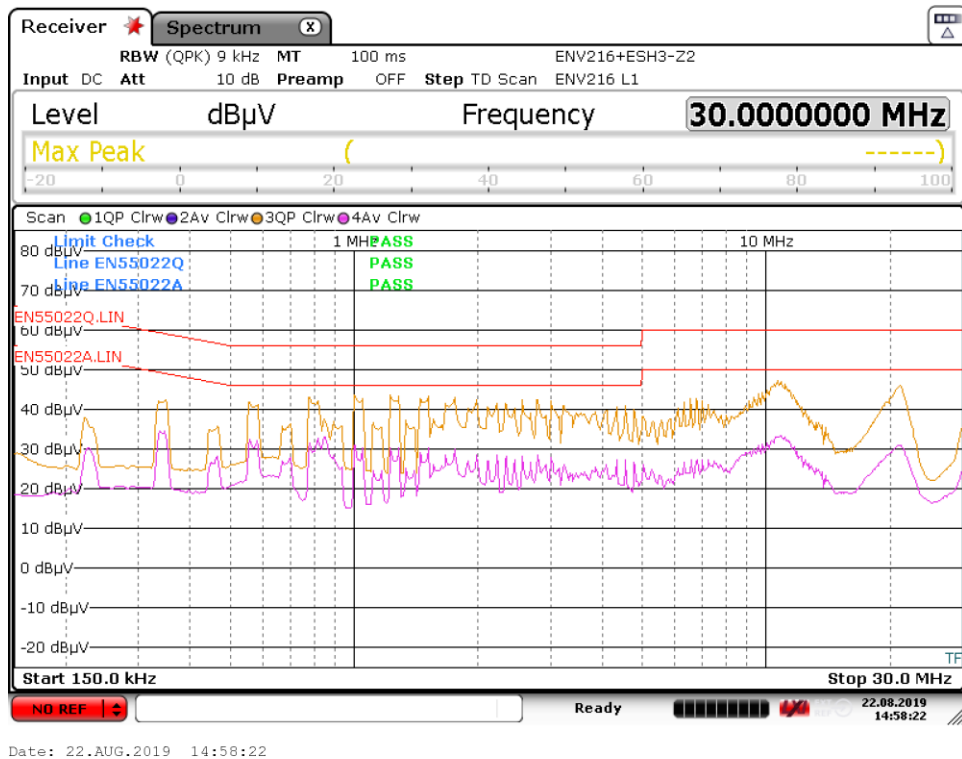


Figure 65 – Conducted EMI, 230 VAC, 9 Ω Floating Load.



17 Revision History

Date	Author	Revision	Description and Changes	Reviewed
06/21/19	RH	1	First Draft	
11/14/19	RH	2	2 nd Draft with added figures	
01/23/20	RH	3	Test mods, added pictures	

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