# 2SP0430T2xxC
# SCALE-2™ Family

Plug-and-Play Gate Driver for Driving
PrimePACK™ 3+ Power Modules
via Electrical Interface

## Product Highlights

### Highly Integrated, Compact Footprint

- Ready-to-use gate driver solution for PrimePACK™ 3+ IGBT power modules with up to 2300 V blocking voltage
- Dual channel gate driver
- Electrical interface
- Secondary side power supply with reinforced isolation
- ±30 A peak output gate current
- 2 W output power per channel at maximum ambient temperature
- -40 °C to 85 °C operating ambient temperature

### Protection / Safety Features

- Short-circuit protection
- Dynamic Advanced Active Clamping (DA²C) for 2SP0430T2A0C and 2SP0430T2B0C gate drivers
- Advanced Active Clamping (AAC) for 2SP0430T2D0C
- Reinforced insulation between primary and secondary side
- Undervoltage lock-out (UVLO) protection for primary side (low voltage side) and secondary-side (high voltage side)
- Applied double sided conformal coating

### Full Safety and Regulatory Compliance

- 100% production partial discharge and HIPOT test of transformer
- Clearance and creepage distances between primary and secondary sides meet requirements for reinforced isolation
- RoHS compliant

## Applications

- Wind and PV power
- Traction inverter
- Industrial drives
- Other industrial applications

## Description

The plug-and-play 2SP0430T2xxC gate driver family is a compact double-channel intelligent gate driver designed for operation of up to 2300 V PrimePACK™ 3+ power modules in 2-level and 3 level applications.

It features an electrical interface and a built-in DC/DC power supply with reinforced isolation. An enhanced level of protection is provided by implemented short-circuit monitoring.

Power Integrations' Dynamic Advanced Active Clamping allows an extended DC-link voltage range in IGBT off-state for up to 60 s. It is implemented in 2SP0430T2A0C and 2SP0430T2B0C gate driver versions, while 2SP0430T2D0C has Advanced Active Clamping (AAC) feature.

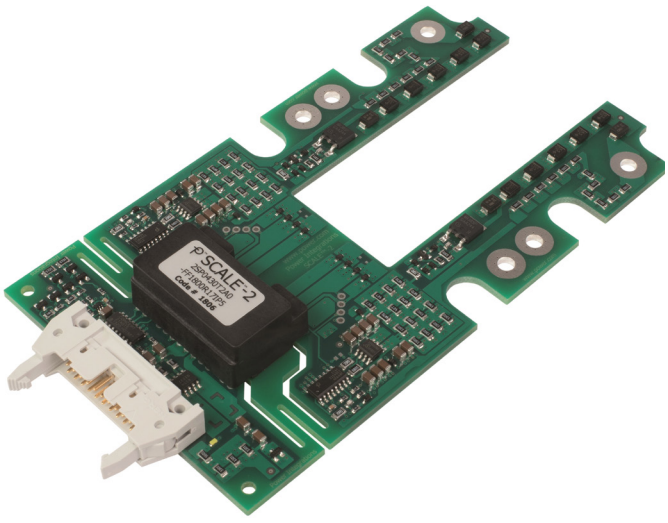


Figure 1. Board Photo of 2SP0430T2A0C.

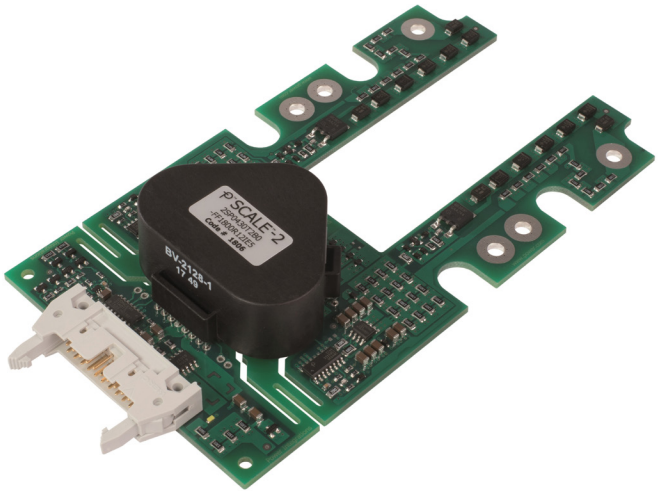


Figure 2. Board Photo of 2SP0430T2B0C (The 2SP0430T2D0C is similar with minor differences in the layout).

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## Pin Functional Description

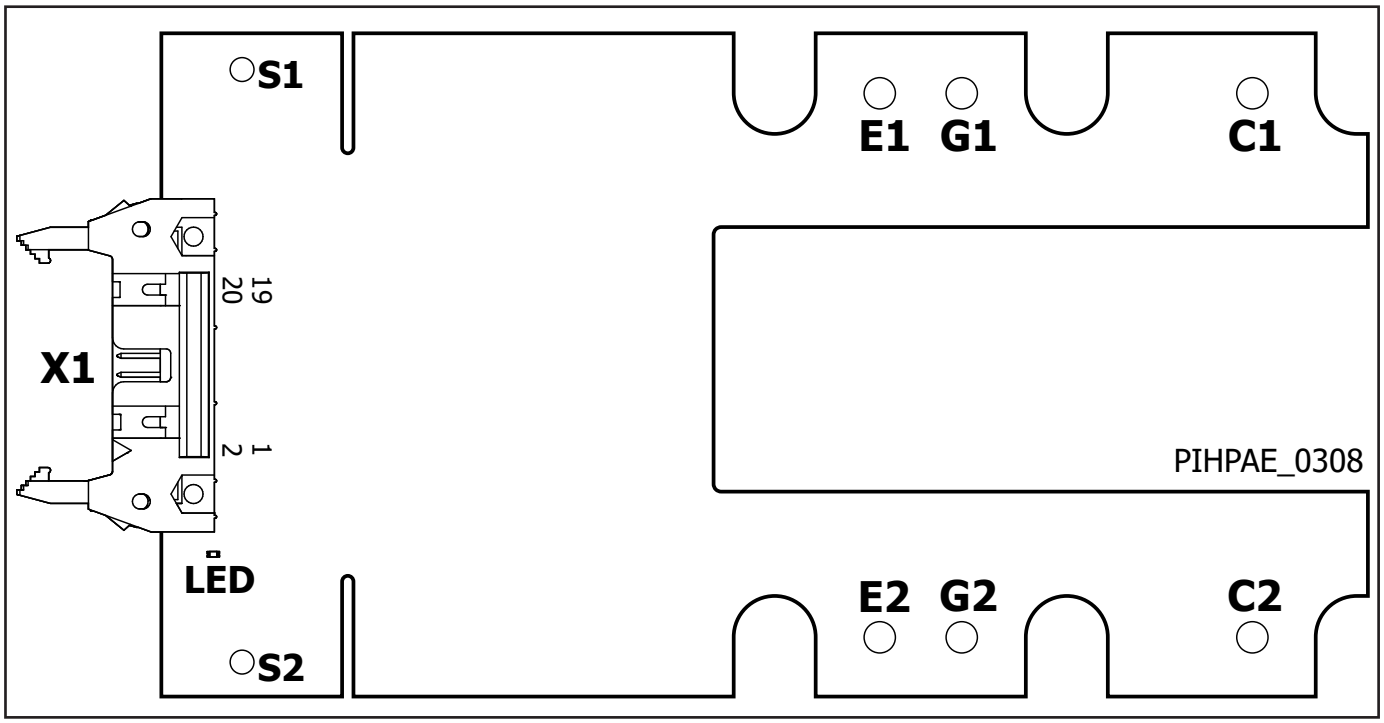


Figure 3. Pin Configuration.

### Connections to Power Module

Connections by screws to the power module.

**E1**
Auxiliary emitter contact of channel 1 switch.

**G1**
Gate contact of channel 1 switch.

**C1**
Auxiliary collector contact of channel 1 switch.

**E2**
Auxiliary emitter contact of channel 2 switch.

**G2**
Gate contact of channel 2 switch.

**C2**
Auxiliary collector contact of channel 2 switch.

### Fixation Holes S1, S2

M3 holes for fixation points of stand-offs.

### Connector X1

To superior controller (FCI 71922-120LF from Amphenol FCI or similar).

**VDC (Pins 1, 3)**
These pins are the primary-side 15 V supply voltage connection for the integrated DC/DC converter. It is mandatory to use the same supply for VDC and VCC.

**VCC (Pins 5, 7)**
These pins are the primary-side 15 V supply voltage connection for the primary-side electronic. It is mandatory to use the same supply for VDC and VCC.

**IN1 (Pin 15)**
This pin is the command input for channel 1.

**SO1 (Pin 13)**
This pin is the command status output for channel 1.

**IN2 (Pin 11)**
This pin is the command input for channel 2.

**SO2 (Pin 9)**
This pin is the command status output for channel 2.

**GND (Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20)**
These pins are the connection for the primary-side ground potential. All primary-side signals refer to these pins.

### Optical Indicator

**LED**

White optical indicator for monitoring the voltage $V_{VCC}$. During the absence of $V_{VCC}$ the indicator is OFF.

## Functional Description

The basic topology of the 2SP0430T2xxC driver is shown in Figure 4. The 2SP0430T2xxC is a dual-channel plug-and-play gate driver for PrimePACK™ 3+ power modules. It is available in different variants, which all provide reinforced isolation for all primary-side signals. The 2SP0430T2A0C features an isolation rating between the primary and secondary sides of 5000 $V_{RMS}$, while the 2SP0430T2B0C and 2SP0430T2D0C feature isolation ratings of 9100 $V_{RMS}$. As plug-and-play gate drivers, the 2SP0430T2xxC characteristics match the requirements of the individual power modules.

The operation of channel 1 (low-side switch) and channel 2 (high-side switch) of the gate driver is independent from each other. Any dead time insertion, to avoid synchronous or overlapping switching of the driven power switches, has to be generated in the external system controller.
Note: Synchronous or overlapping switching of top and bottom switches within a half-bridge leg may damage or destroy the driven power switch(es) and, in conjunction as secondary failure, the attached gate driver.

### Power Supply

The 2SP0430T2xxC provides two power supply inputs. For both a typical supply voltage level of 15 V is required. The first input VDC supplies the integrated DC/DC converter, which generates the isolated voltage for the secondary-side gate driver channels. The positive rail of the gate driver channels has the voltage level $V_{VISO}$ and the negative rail has the voltage level $V_{COM}$. Both are referenced to the emitter potential at terminal E1 or E2 of the driven power semiconductor.
The second input VCC supplies the primary-side electronic of the gate driver. It is mandatory to supply VDC and VCC from the same source.

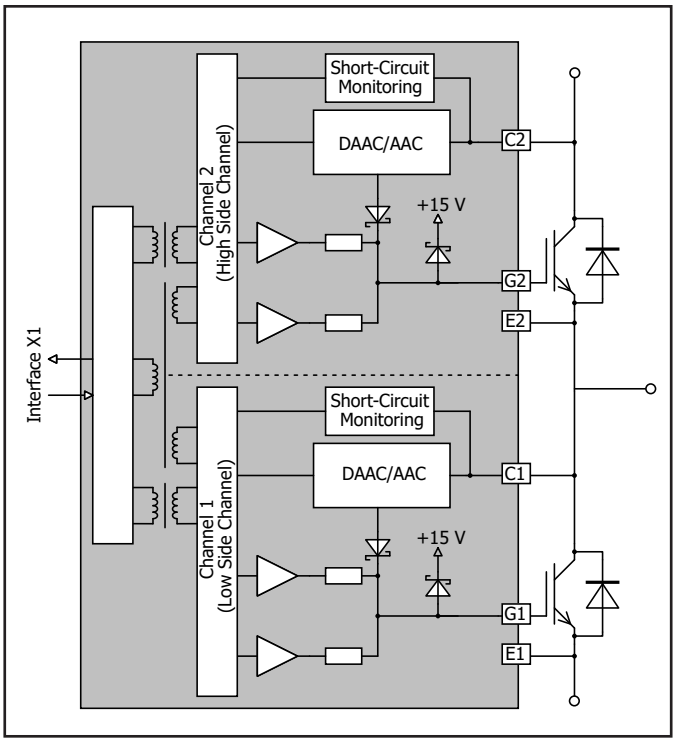


Figure 4. Functional Block Diagram of 2SP0430T2xxC

### Under Voltage Monitoring

The supply voltages are closely monitored. In case of an under voltage condition (UVLO), a failure signal will be provided on the status output SO1/SO2 of the gate driver. If the UVLO is present on the primary-side supply, both status output signals will be set to GND and all gate driver channels will be turned off synchronously. In case of an UVLO on the secondary-side, the status signal of the respective channel will be set to GND and the corresponding power semiconductor will be turned off.

### Signal Input (Primary-Side X1)

The input logic of IN1 and IN2 is designed to work with 15 V logic levels to provide a sufficient signal/noise ratio. Both inputs have positive logic and are edge-triggered.

Gate driver signals are transferred from the IN1 and IN2 pins to the gate with a propagation delay of $t_{P(LH)}$ for the turn-on and $t_{P(HL)}$ for the turn-off commands.

### Status Output (Primary-Side X1)

The gate driver provides status feedbacks SO1 and SO2. The status feedback signals SO1 and SO2 stay at $V_{VCC}$ under no-fault conditions. In case of a fault, e.g. detected short-circuit of the driven power module or an under voltage lock-out (UVLO) condition on the secondary-side, the status feedback is set to GND potential for a duration of $t_{BLK}$. In the case of a primary-side UVLO condition, both status feedback signals remain at GND during the UVLO and are extended by $t_{BLK}$. During this time, no gate signals will be transmitted to the respective gate driver channel.

### Gate Voltage

2SP0430T2xxC possesses a voltage regulator for the positive (turn-on) rail of the gate voltage. Internal current sources are regulating actively the positive gate-emitter voltage independently of actual load conditions within the maximum specified ratings. Therefore, the on-state gate-emitter voltage $V_{GE(on)}$ of the power semiconductor equals in steady state the positive supply voltage $V_{VISO}$.

The off-state gate-emitter voltage $V_{GE(off)}$ equals in steady state the voltage $V_{COM}$. This voltage is load-dependent. It has its lowest value under no-load conditions and is increasing slightly (i.e. getting less negative) with increasing load.

In the event of an under voltage lock-out condition the gate driver changes the control of the positive rail towards the control of the negative rail $V_{COM}$. By this potential parasitic turn-on events of the power semiconductor are avoided.

### Short-Circuit Protection

The gate driver uses the semiconductor desaturation effect to detect short-circuits. The desaturation is monitored by using a resistive sensing network. At turn-on, the collector-emitter voltage is checked after the response time $t_{RES}$ to detect a short circuit. If the voltage is higher than the programmed threshold voltage $V_{CE(SAT)}$, the driver detects a short-circuit condition. The monitored semiconductor is switched off immediately and a fault signal is transmitted to status output SO1/SO2 after the delay $t_{SOx}$.

The fault feedback is automatically reset after the blocking time $t_{BLK}$. The semiconductor is turned on again as soon as the next positive edge is applied to the respective inputs IN1 or IN2 after the fault status of the corresponding channel has disappeared. It should be noted that the response time $t_{RES}$ is dependent on the DC-link voltage. It remains constant between about 50% to 100% of the maximum DC-link voltage and increases at lower DC-link voltages.

### Screw Terminals S1, S2

The gate driver is mounted on top of the power module and fixed by screws. Details are given in the Mounting Instruction Section.

## Gate Clamping

In the event of a short-circuit condition, the gate voltage is increased due to the high $dv_{CE}/dt$ between the collector and emitter terminals of the driven power semiconductor. This $dv_{CE}/dt$ drives a current through the Miller-capacitance (capacitance between the gate and collector) and charges the gate capacitance, which eventually leads to a gate-emitter voltage larger than the nominal gate-emitter turn-on voltage. In consequence, the short-circuit current is increased due to the transconductance of the power semiconductor. To ensure that the gate-emitter voltage stays close to the nominal turn-on voltage, each driver features gate-clamping circuitry. The gate clamping provides a voltage similar to $V_{VISO}$ to the gate, i.e. 15 V. As the effective short-circuit current is a function of the gate-emitter voltage the short-circuit current is limited. This is shown in Figure 4 where the gate-emitter voltage and in consequence the short-circuit current is kept at a flat plateau. As consequence, the energy dissipated in the power semiconductor during the short-circuit event is reduced, leading to a junction temperature within the short-circuit safe operating area (SCSOA) limits and enabling a safe turn-off of the device.

## Dynamic Advanced Active Clamping (DA²C)

Active clamping acts to partially turn on the IGBT in the event that the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic active clamping topologies implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate. The gate drivers 2SP0430T2A0C and 2SP0430T2B0C contain Power Integrations' Dynamic Advanced Active Clamping (DA²C), while 2SP0430T2D0C has the Advanced Active Clamping (AAC). They operate as follows:

When active clamping is activated, the turn-off MOSFET for the gate driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature is called Advanced Active Clamping (AAC).

Additional TVS diodes have been added in series to the TVS diodes required to withstand the maximum DC-link voltage under non-switching operation on 2SP0430T2A0C and 2SP0430T2B0C. These TVS diodes are short-circuited during the IGBT on-state as well as for about 15…20 µs after the turn-off command to guarantee efficient active clamping. After this delay, these additional TVS diodes are activated and allow the DC-link voltage to be increased to a higher value during the IGBT off-state. This feature, illustrated in Figure 5 – together with Advanced Active Clamping – is called Dynamic Advanced Active Clamping (DA²C). The time during which the voltage can be applied above the value for switching operation has to be limited to short periods (< 60 s).

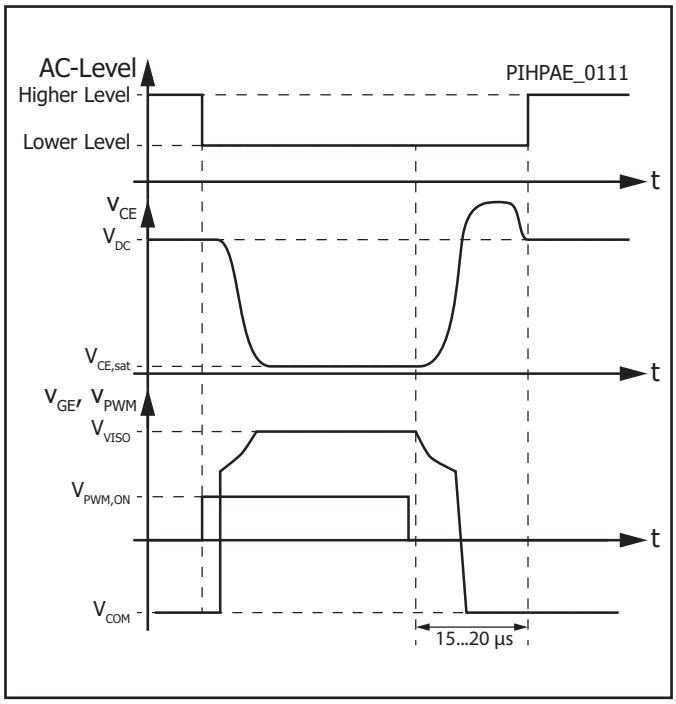


Figure 5. Dynamic Advanced Active Clamping (DA²C).

## Conformal Coating

The electronic components of the gate driver are protected by a layer of acrylic conformal coating with a typical thickness of 50 µm using ELPEGUARD SL 1307 FLZ/2 from Lackwerke Peters on both sides of the PCB. This coating layer increases the product reliability when exposed to contaminated environments.

Note: Standing water (e.g. condensate water) on top of the coating layer is not allowed as this water will diffuse over time through the layer. Eventually, it will form a thin film of conducting nature between PCB surface and coating layer, which will cause leakage currents. Such currents may lead to a reduction of the performance of the gate driver.

## Absolute Maximum Ratings

| Parameter | Symbol | Conditions $T_A$ = -40 °C to 85 °C | | Min | Max | Units |
|---|---|---|---|---|---|---|
| **Absolute Maximum Ratings[1]** | | | | | | |
| **Primary-Side Supply Voltage** | $V_{VDC}$ | VDC and VCC to GND | | 0 | 16 | V |
| | $V_{VCC}$ | | | 0 | 16 | |
| **Primary-Side Supply Current** | $I_{VDC}$ | Average supply current at full load | | | 480 | mA |
| | $I_{VCC}$ | Average supply current at full load | | | 45 | |
| **Logic Input Voltage (Command Signal)** | $V_{INx}$ | INx to GND, low-state | | 0 | 4 | V |
| | | INx to GND, high-state | | 12.6 | $V_{VCC}$ +0.5 | |
| **Logic Output Voltage (Status Signal)** | $V_{SOx}$ | SOx to GND | | 0 | $V_{VCC}$ +0.5 | V |
| **Switching Frequency[2]** | $f_{SW}$ | | | | 10 | kHz |
| **Gate Output Power Per Channel** | $P_{GX}$ | | | | 2 | W |
| **Primary to Secondary Side Operating Voltage** | $V_{OP,PS}$ | 2SP0430T2A0C | Transient only | | 1700 | V |
| | | | Permanently applied | | 1250 | |
| | | 2SP0430T2B0C | Transient only | | 2050 | |
| | | | Permanently applied | | 1500 | |
| | | 2SP0430T2D0C | Transient only | | 2300 | |
| | | | Permanently applied | | 1600 | |
| **DC-Link Voltage** | $V_{DC-Link}$ | Switching operation[3] (2.3 kV driver versions) | | | 1600 | $V_{DC}$ |
| | | Off State[3] (2.3 kV driver versions) | | | 1600 | |
| | | Switching operation[3] (1.7 kV driver versions) | | | 1250 | |
| | | Off State[4] (1.7 kV driver versions) | | | 1500 | |
| | | Switching operation[3] (1.2 kV driver versions) | | | 850 | |
| | | Off State[4] (1.2 kV driver versions) | | | 1100 | |
| **Test Voltage Primary-Side to Secondary-Side** | $V_{ISO(PS)}$ | 50 Hz, 60 s (2SP0430T2B0C and 2SP0430T2D0C) | | | 9100 | $V_{RMS}$ |
| | | 50 Hz, 60 s (2SP0430T2A0C) | | | 5000 | |
| **Test Voltage Secondary-Side to Secondary-Side** | $V_{ISO(SS)}$ | 50 Hz, 60 s (2SP0430T2B0C and 2SP0430T2D0C) | | | 6000 | $V_{RMS}$ |
| | | 50 Hz, 60 s (2SP0430T2A0C) | | | 4000 | |
| **Common-Mode Transient Immunity** | \|dv/dt\| | | | | 50 | kV/µs |
| **Storage Temperature[5]** | $T_{ST}$ | | | -40 | 50 | °C |
| **Operating Ambient Temperature** | $T_A$ | | | -40 | 85 | °C |
| **Surface Temperature[6]** | T | | | | 125 | °C |
| **Relative Humidity** | $H_R$ | No condensation | | | 93 | % |
| **Altitude of Operation[7]** | $A_{OP}$ | | | | 2000 | m |

## Recommended Operating Conditions

| Parameter | Symbol | Conditions<br>$T_A$ = -40 °C to 85 °C | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| **Supply Voltage** | $V_{VDC}$ | VDC to GND | 14.5 | 15 | 15.5 | V |
| | $V_{VCC}$ | VCC to GND | 14.5 | 15 | 15.5 | |

## Characteristics

| Parameter | Symbol | Conditions<br>$V_{VDC}$ = $V_{VCC}$ = 15 V, $T_A$ = 25 °C | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | | |
| **Supply Current** | $I_{VDC}$ | | Without load (2SP0430T2A0C) | | 32 | | mA |
| | | | Without load (2SP0430T2B0C and 2SP0430T2D0C) | | 65 | | |
| | | | $P_G$ = $P_{G,max}$ (2SP0430T2A0C) | | 344 | | |
| | | | $P_G$ = $P_{G,max}$ (2SP0430T2B0C and 2SP0430T2D0C) | | 384 | | |
| | $I_{VCC}$ | | 2SP0430T2A0C | | 37 | | |
| | | | 2SP0430T2B0C and 2SP0430T2D0C | | 32 | | |
| **Power Supply Monitoring Threshold (Primary Side)** | $UVLO_{VCC}$ | Referenced to GND | Clear fault (resume operation) | 11.6 | 12.6 | 13.6 | V |
| | | | Set fault (suspend peration) | 11.0 | 12.0 | 13.0 | |
| | | | Hysteresis | 0.35 | | | |
| **Power Supply Monitoring Threshold (Secondary Side)** | $UVLO_{VISO}$ | Referenced to E | Clear fault (resume operation) | 11.6 | 12.6 | 13.6 | V |
| | | | Set fault (suspend peration) | 11.0 | 12.0 | 13.0 | |
| | | | Hysteresis | 0.35 | | | |
| | $UVLO_{COM}$ | | Clear fault (resume operation) | | -5.15 | | V |
| | | | Set fault (suspend peration) | | -4.85 | | |
| | | | Hysteresis | | 0.3 | | |
| **Output Voltage (Secondary Side)** | $V_{VISO-COM}$ | | Without load (2SP0430T2A0C) | | 25.9 | | V |
| | | | Without load (2SP0430T2B0C and 2SP0430T2D0C) | | 24.6 | | |
| | | | $P_G$ = $P_{G,max}$ (2SP0430T2A0C) | | 24.8 | | |
| | | | $P_G$ = $P_{G,max}$ (2SP0430T2B0C and 2SP0430T2D0C) | | 24.0 | | |
| **Coupling Capacitance** | $C_{io}$ | Primary-side to secondary-side, total per channel (2SP0430T2A0C) | | | 22 | | pF |
| | | Primary-side to secondary-side, total per channel (2SP0430T2B0C and 2SP0430T2D0C) | | | 19 | | |

## Characteristics (cont.)

| Parameter | Symbol | Conditions<br>$V_{VDC}$ = $V_{VCC}$ = 15 V, $T_A$ = 25 °C | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Timing Characteristics** | | | | | | |
| **Turn-On Delay** | $t_{P(LH)}$ | 50% of INx to 50% of $V_{GE(on)}$, no load attached | | 215 | | ns |
| **Turn-Off Delay** | $t_{P(HL)}$ | 50% of INx to 50% of $V_{GE(off)}$, no load attached | | 145 | | ns |
| **Transmission Delay of Fault State** | $t_{SOx}$ | Delay from fault detection to SOx | | 450 | | ns |
| **Blocking Time** | $t_{BLK}$ | Delay to clear fault state | | 98 | | ms |
| **Logic Inputs and Status Outputs** | | | | | | |
| **Input Impedance** | $R_{INx}$ | | 4.4 | 4.5 | 4.6 | kΩ |
| **Turn-On Threshold** | $V_{TH-ON(INx)}$ | INx to GND | | 10.1 | | V |
| **Turn-Off Threshold** | $V_{TH-OFF(INx)}$ | INx to GND | | 6.4 | | V |
| **Status Output Voltage** | $V_{SOx}$ | No fault condition, SOx current ≤ 0.5 mA | 11 | | | V |
| **SOx Pull-Up Resistor to VCC** | $R_{SOx}$ | On the driver board | | 6.8 | | kΩ |
| **Gate Output** | | | | | | |
| **Gate Turn-on Voltage** | $V_{GE(on)}$ | Without load | | 15 | | V |
| | | $P_G$ = $P_{G,max}$ | | 15 | | |
| **Gate Turn-off Voltage** | $V_{GE(off)}$ | Without load<br>(2SP0430T2A0C) | | -10.9 | | V |
| | | Without load<br>(2SP0430T2B0C and 2SP0430T2D0C) | | -9.6 | | |
| | | $P_G$ = $P_{G,max}$<br>(2SP0430T2A0C) | | -9.8 | | |
| | | $P_G$ = $P_{G,max}$<br>(2SP0430T2B0C and 2SP0430T2D0C) | | -9.0 | | |

## Characteristics (cont.)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Short-Circuit Protection** | | | | | | | |
| **Static $V_{CE}$-Monitoring Threshold** | $V_{CE(SAT)}$ | 2.3 kV driver versions | | | 68 | | V |
| | | 1.7 kV driver versions | | | 54 | | |
| | | 1.2 kV driver versions | | | 47 | | |
| **Response Time** | $t_{RES}$ | 10% to 90% of $V_{GE}$ (2.3 kV versions) | DC-link voltage = 1600 V | | 3.5 | | µs |
| | | | DC-link voltage = 1200 V | | 3.6 | | |
| | | | DC-link voltage = 800 V | | 4.5 | | |
| | | | DC-link voltage = 600 V | | 5.8 | | |
| | | 10% to 90% of $V_{GE}$ (1.7 kV versions) | DC-link voltage = 1250 V | | 7.0 | | |
| | | | DC-link voltage = 1000 V | | 7.1 | | |
| | | | DC-link voltage = 800 V | | 7.4 | | |
| | | | DC-link voltage = 600 V | | 8.2 | | |
| | | 10% to 90% of $V_{GE}$ (1.2 kV versions) | DC-link voltage = 800 V | | 6.8 | | |
| | | | DC-link voltage = 600 V | | 7.5 | | |
| | | | DC-link voltage = 400 V | | 8.0 | | |
| | | | DC-link voltage = 300 V | | 9.3 | | |
| **Electrical Isolation** | | | | | | | |
| **Test Voltage (50Hz/1s)[8]** | $V_{ISO(PS)}$ | Primary to secondary side (2SP0430T2A0C) | | 5000 | | | $V_{RMS}$ |
| | | Primary to secondary side (2SP0430T2B0C and 2SP0430T2D0C) | | 9100 | | | |
| | $V_{ISO(SS)}$ | Secondary to secondary side (2SP0430T2A0C) | | 4000 | | | |
| | | Secondary to secondary side (2SP0430T2B0C and 2SP0430T2D0C) | | 6000 | | | |
| **Partial Discharge Extinction Voltage[9]** | $PD_{P-S}$ | Primary to secondary side (2SP0430T2A0C) | | 1768 | | | $V_{pk}$ |
| | | Primary to secondary side (2SP0430T2B0C and 2SP0430T2D0C) | | 3450 | | | |
| | $PD_{S-S}$ | Secondary side to secondary side (2SP0430T2A0C) | | 1700 | | | |
| | | Secondary side to secondary side (2SP0430T2B0C and 2SP0430T2D0C) | | 2875 | | | |

## Characteristics (cont.)

| | | | | | | |
|---|---|---|---|---|---|---|
| **Creepage Distance** | $CPG_{P-S}$ | Primary side to secondary side, on the PCB, material group IIIa (2SP0430T2A0C and 2SP0430T2B0C) | 30 | | | mm |
| | | Primary side to secondary side, on the PCB, material group IIIa (2SP0430T2D0C) | 30 | | | |
| | $CPG_{S-S}$ | Secondary side to secondary side, on the PCB, material group IIIa (2SP0430T2A0C and 2SP0430T2B0C) | 7 | | | |
| | | Secondary side to secondary side, on the PCB, material group IIIa (2SP0430T2D0C) | 15 | | | |
| **Clearance Distance** | $CLR_{P-S}$ | Primary side to secondary side (2SP0430T2A0C and 2SP0430T2B0C) | 12.6 | | | mm |
| | | Primary side to secondary side (2SP0430T2D0C) | 12.6 | | | |
| | $CLR_{S-S}$ | Secondary side to secondary side (2SP0430T2A0C and 2SP0430T2B0C) | 7 | | | |
| | | Secondary side to secondary side (2SP0430T2D0C) | 7.4 | | | |
| **Mounting**[10] | | | | | | |
| **Connection Torque** | $M_{Terminal}$ | Terminals (Cx, Gx and Ex), M4 screw | 1.8 | | 2.1 | Nm |
| **Mounting Holes** | $D_{Hole}$ | Diameter of screw holes S1, S2 | | 3.2 | | mm |
| | | Diameter of screw holes Cx, Gx and Ex | | 4.4 | | |
| **Bending** | $I_{bend}$ | According to IPC | | | 0.75 | % |

## Mounting Instruction

The driver is mounted on top of the target power module. 2SP0430T2xxC must be screwed to the power semiconductor module with metal screws. The mounting force is given with $M_{Terminal}$. $M_{Terminal}$ must not exceed the values given in the respective data sheet of the target power module. Hence, the actual mounting torque may be smaller than $M_{Terminal}$. It is recommended to follow mounting instructions from the corresponding power semiconductor manufacturer.

To ensure proper cooling by natural or forced convection minimum clearance of 50 mm of the driver top side is required. This includes also that the AC and/or DC bus bars are not covering parts or the entire driver top side.

NOTES:

1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
2. This limit applies to the whole product family. The actual achievable switching frequency may be lower for specific gate driver variants and has to be validated in final system as it is additionally limited by maximum gate output power in conjunction with the maximum allowed surface temperature.
3. This limit is due to active clamping.
4. Due to the Dynamic Active Advanced Clamping Function ($DA^2C$) implemented on the driver, the DC link voltage can be increased in the off state condition (e.g. after emergency shutdown). This value is only valid when the IGBTs are in the off state (not switching). The time during which the voltage can be applied should be limited to short periods (< 60 seconds).
5. The storage temperature inside the original package or in case the coating material of coated products may touch external parts must be limited to the given value. Otherwise, it is limited to 85°C.
6. The component surface temperature, which may strongly vary depending on the operating condition, must be limited to the given value to ensure long-term reliability of the product.
7. Operation above this level requires a voltage derating to ensure proper isolation coordination.
8. The transformer of every production sample has undergone 100% testing at the given value or higher for 1s.
9. Partial discharge measurement is performed on each transformer.
10. Refer to the data sheet of the IGBT module.

## Product Dimensions

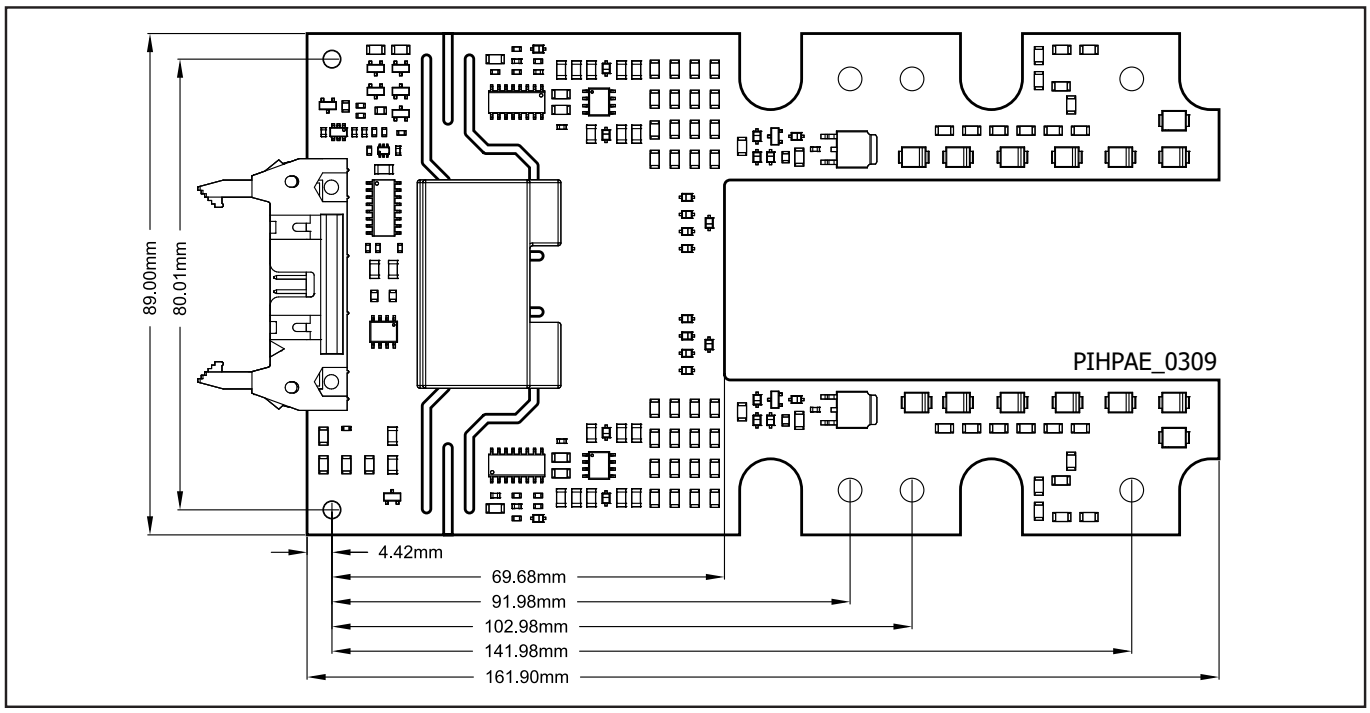


Figure 6. Top View of 2SP0430T2A0C

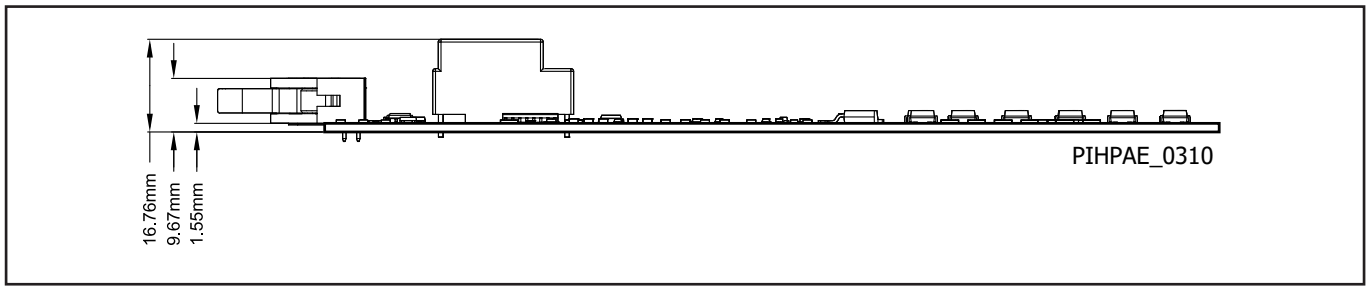


Figure 7. Side View of 2SP0430T2A0C.

## Product Dimensions

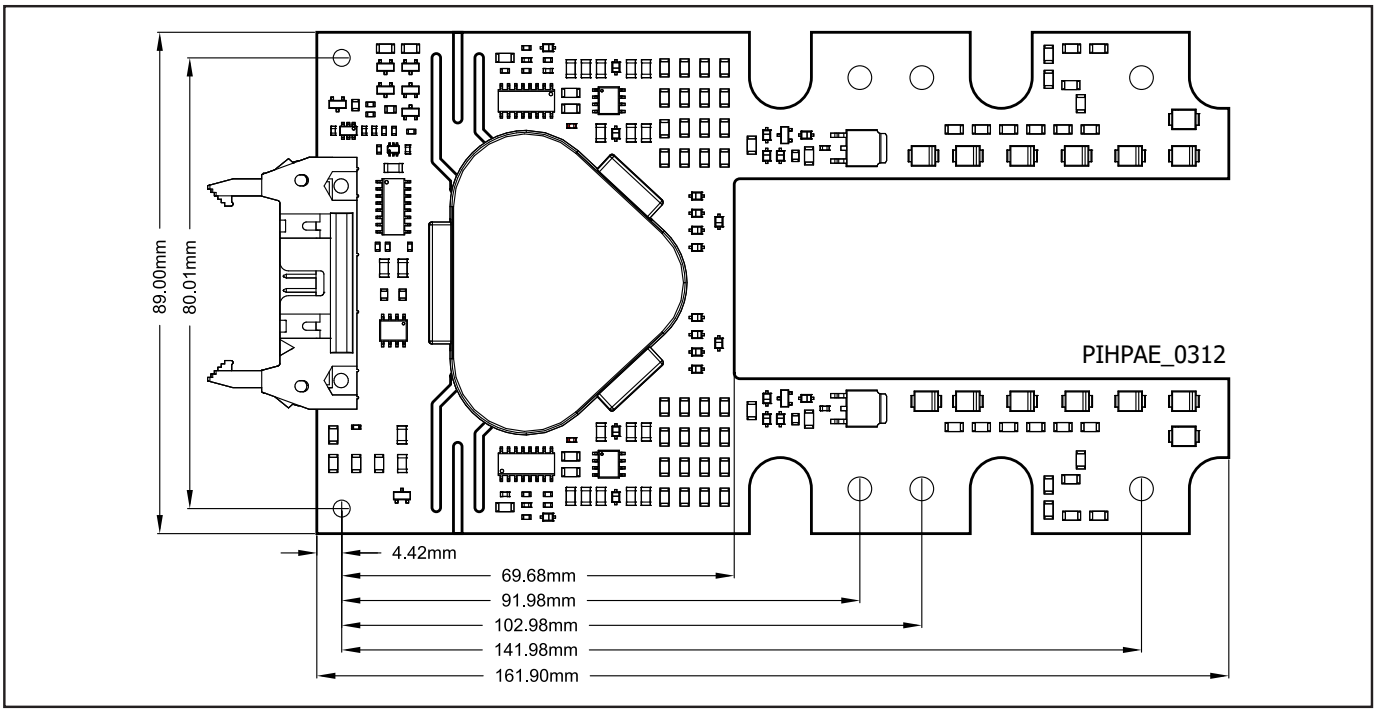


Figure 8. Top View of 2SP0430T2B0C

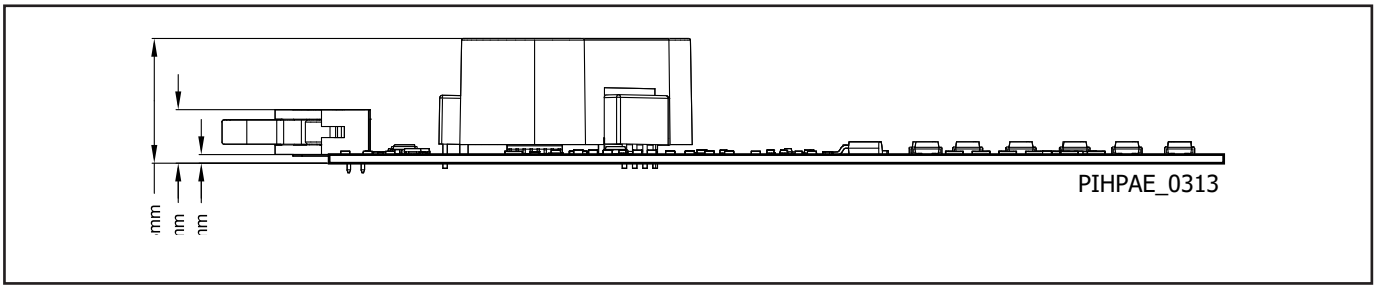


Figure 9. Side View of 2SP0430T2B0C.

## Product Dimensions

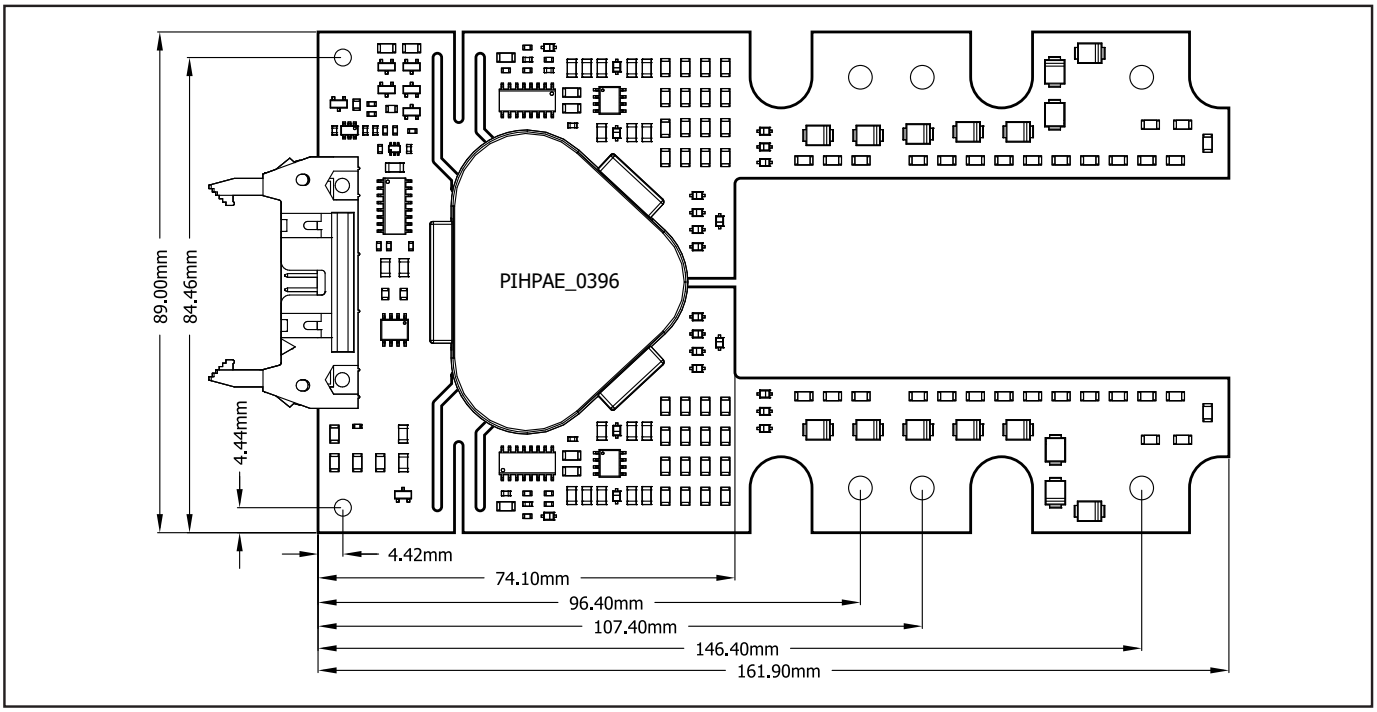


Figure 10. Top View of 2SP0430T2D0C

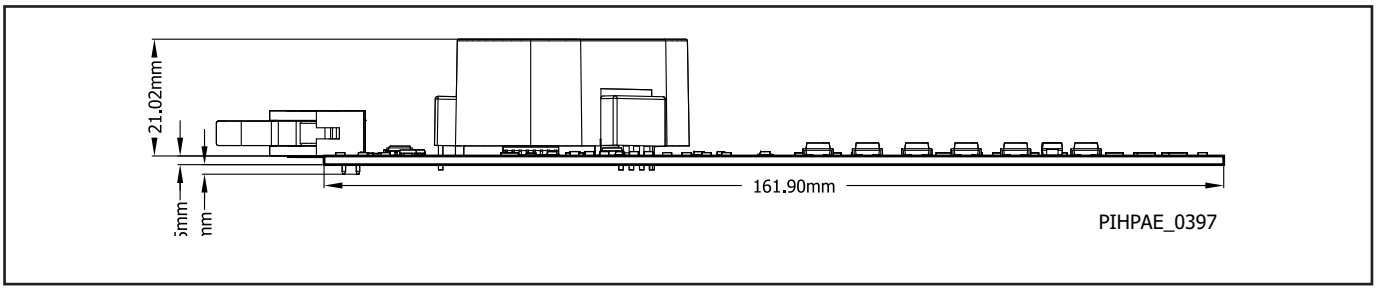


Figure 11. Side View of 2SP0430T2D0C.

## Transportation and Storage Conditions

For transportation and storage conditions refer to Power Integrations' Application Note AN-1501.

## RoHS Statement

We hereby confirm that the product supplied does not contain any of the restricted substances according to Article 4 of the RoHS Directive 2011/65/EU in excess of the maximum concentration values tolerated by weight in any of their homogeneous materials.

Additionally, the product complies with RoHS Directive 2015/863/EU (known as RoHS 3) from 31 March 2015, which amends Annex II of Directive 2011/65/EU.

## Product details

| Part Number | Power Module | Voltage Class | Current Class | Package | IGBT Supplier | $R_{G(on)}$ | $R_{G(off)}$ |
|---|---|---|---|---|---|---|---|
| **2SP0430T2D0C-FF1800R23IE7** | FF1800R23IE7 | 2300 V | 1800 A | PrimePACK™ 3+ | Infineon | 0.0 Ω | 4.0 Ω |
| **2SP0430T2A0C-FF1800R17IP5** | FF1800R17IP5 | 1700 V | 1800 A | PrimePACK™ 3+ | Infineon | 0.5875 Ω | 5.875 Ω |
| **2SP0430T2B0C-FF1800R17IP5** | FF1800R17IP5 | 1700 V | 1800 A | PrimePACK™ 3+ | Infineon | 0.5875 Ω | 5.875 Ω |
| **2SP0430T2A0C-2MBI1800XXG170-50** | 2MBI1800XXG170-50 | 1700 V | 1800 A | PrimePACK™ 3+ | Fuji | 0.225 Ω | 3.375 Ω |
| **2SP0430T2B0C-2MBI1800XXG170-50** | 2MBI1800XXG170-50 | 1700 V | 1800 A | PrimePACK™ 3+ | Fuji | 0.225 Ω | 3.375 Ω |
| **2SP0430T2A0C-FF1500R17IP5** | FF1500R17IP5 | 1700 V | 1500 A | PrimePACK™ 3+ | Infineon | 0.5875 Ω | 7.0 Ω |
| **2SP0430T2B0C-FF1500R17IP5** | FF1500R17IP5 | 1700 V | 1500 A | PrimePACK™ 3+ | Infineon | 0.5875 Ω | 7.0 Ω |
| **2SP0430T2A0C-FF2400R12IP7** | FF2400R12IP7 | 1200 V | 2400 A | PrimePACK™ 3+ | Infineon | 0.2 Ω | 2.5 Ω |
| **2SP0430T2B0C-FF2400R12IP7** | FF2400R12IP7 | 1200 V | 2400 A | PrimePACK™ 3+ | Infineon | 0.2 Ω | 2.5 Ω |
| **2SP0430T2A0C-FF1800R12IE5** | FF1800R12IE5 | 1200 V | 1800 A | PrimePACK™ 3+ | Infineon | 0.85 Ω | 3.375 Ω |
| **2SP0430T2B0C-FF1800R12IE5** | FF1800R12IE5 | 1200 V | 1800 A | PrimePACK™ 3+ | Infineon | 0.85 Ω | 3.375 Ω |
| **2SP0430T2A0C-FF1500R12IE5** | FF1500R12IE5 | 1200 V | 1500 A | PrimePACK™ 3+ | Infineon | 0.85 Ω | 3.375 Ω |
| **2SP0430T2B0C-FF1500R12IE5** | FF1500R12IE5 | 1200 V | 1500 A | PrimePACK™ 3+ | Infineon | 0.85 Ω | 3.375 Ω |

| Revision | Notes | Date |
|---|---|---|
| A | Final Datasheet. | 03/24 |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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