Application Note AN-45
LinkSwitch-CV Family

Design Guide

Introduction

The LinkSwitch™-CV family is a highly integrated monolithic switching IC designed for off-line power supplies up to 17 W. Ideally suited for DVD player and Set-top box applications, LinkSwitch-CV provides constant voltage without using an optocoupler or secondary feedback circuitry. ON/OFF control optimizes efficiency across load and line, while meeting no-load and power supply efficiency standards.

Each member of the family has a high-voltage power MOSFET and its controller integrated onto the same die. Internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency modulated (jitter) to reduce EMI. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits the dissipation in the MOSFET, the transformer and the output diode during overload, output short-circuit and open-loop conditions, while the auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault. Power Integrations' EcoSmart™ technology enables supplies designed around the LinkSwitch-CV family members to consume <200 mW of no-load power at 230 VAC without an external bias circuit and down to below <70 mW with a low cost bias circuit. This simplifies meeting harmonized energy efficiency standards.

Basic Circuit Configuration

The circuit shown in Figure 1 shows the basic configuration of a three output flyback power supply designed using LinkSwitch-CV. Because of its high level integration, LinkSwitch-CV leaves far fewer design issues to be addressed externally, resulting in one common circuit configuration for all applications. For example different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged.

Scope

This application note is intended for engineers designing an isolated AC-DC flyback power supply using the LinkSwitch-CV family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To simplify the task this application note refers directly to the PIXls design spreadsheet that is part of the PI Expert™ design software suite. The basic configuration used in LinkSwitch-CV Flyback power supplies is shown in Figure 1.

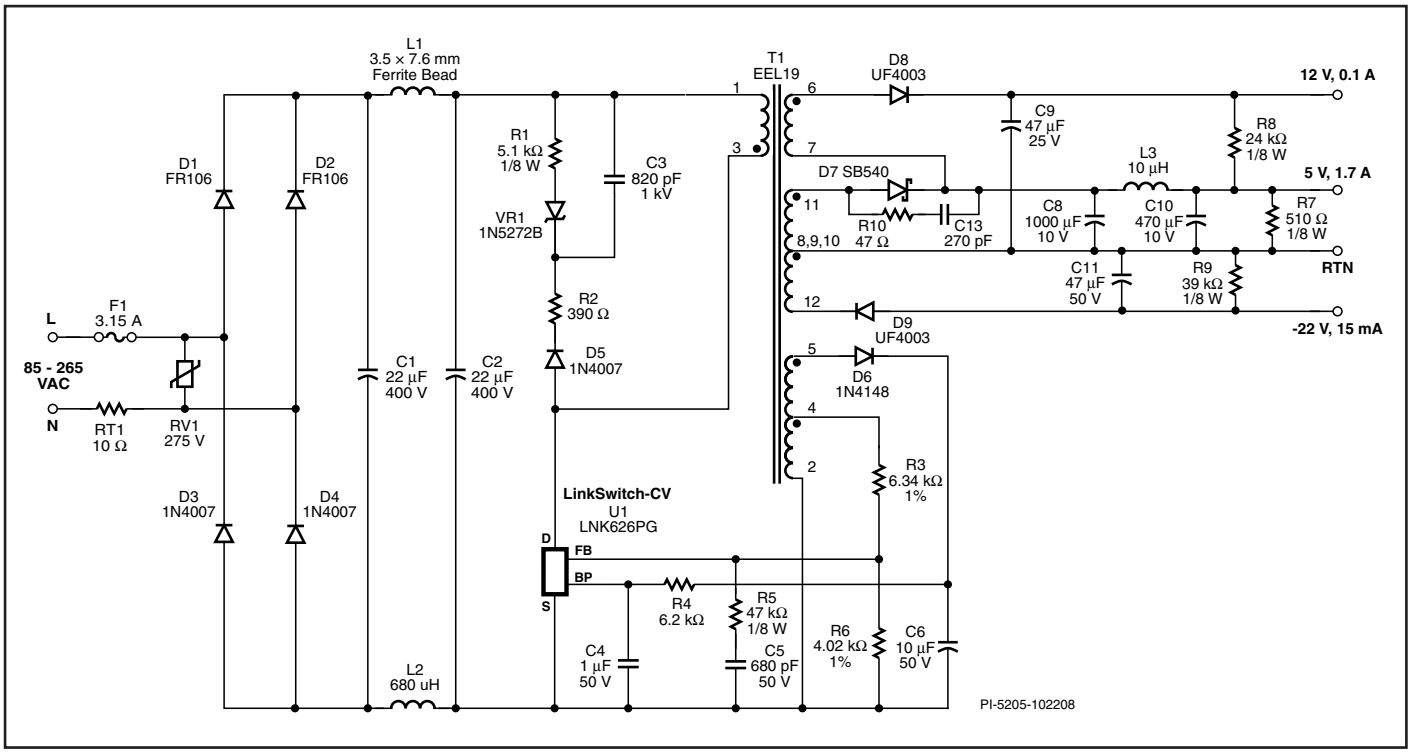


Figure 1. 7 W (10 W peak) Multiple Output Flyback Converter for DVD Applications with Primary Sensed Feedback.

In addition to this application note the reader may also find the LinkSwitch-CV Design Example Report (DER-198) containing the complete design and test data of the DVD power supply in Figure 1. Further details on downloading PI Expert and updates to this document can be found at www.power.com.

Quick Start

Readers who want to start immediately can use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXls spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} and minimum line frequency f_L [B3, B4, B5]
- Enter Nominal Output Voltage V_O [B6], for multiple outputs complete section shown in Figure 13
- Enter the output power value Po [B7]
- Enter efficiency estimate [B8] using Table 1 as guidance

	Universal (85 – 265 VAC)	100/115 VAC (85 – 132 VAC)	230 VAC (185 – 265 VAC)
Single Output (5 V)	0.76	0.76	0.78
Single Output (12 V)	0.80	0.80	0.82
Multiple Output	0.66	0.66	0.68

Table 1. Initial Efficiency Estimates for a New Design.

Adjust the number accordingly after measuring the efficiency of the first prototype-board at peak load and VAC_{MIN}.

- Enter C_{IN} input capacitance [B11]
  - 3 µF/W for universal (85-265 VAC) or single (100/115 VAC) line
  - Use 1 µF/W single 230 VAC for single (195-265 VAC) line
  - Note: After selecting the LinkSwitch-CV device (the step below), if the computed duty cycle [D59] is greater than 54%, increase the input capacitance.
- Select LinkSwitch-CV device from the drop down list or enter directly [B15].
  - Use Table 2 for guidance, selecting a device based on output power, input voltage range and thermal environment (open frame or enclosed adapter).
- Enter V_{DS} [B22], the on-state drain-source voltage drop. Use 10 V if no better data available.
- Enter the output rectifier's forward voltage drop V_D [B23]. Use 0.5 for Schottky and 0.7 for PN diode.
- Enter the core type from the drop down menu. If the desired core is not listed, then you may enter a core's characteristics A_E, L_E and A_L ([B31] [B32] [B33]). Enter the bobbin width BW [B34].
- If margin tape is desired, then enter the margin tape width in [B35]. Note: This will reduce the winding width by two times the margin tape's width.
- Enter the number of primary layers L [B36]. The maximum recommended primary layers is 3.
- If necessary adjust the calculated number of secondary turns N_S [B37] to change the core flux density (BM). Increasing N_S will increase the primary turns and lower BM.

Output Power Table

Product[3]	230 VAC ±15%		85-265 VAC	
	Adapter[1]	Peak or Open Frame[2]	Adapter[1]	Peak or Open Frame[2]
LNK623PG/DG	6.5 W	9 W	5.0 W	6 W
LNK624PG/DG	7 W	11 W	5.5 W	6.5 W
LNK625PG/DG	8 W	13.5 W	6.5 W	8 W
LNK626PG	10.5 W	17 W	8.5 W	10 W

Table 2. Output Power Table. Based on 5 V Output.

Notes:
1. Minimum continuous power in a typical non-ventilated enclosed adapter measured at +50 °C ambient.
2. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient (see Key Application Considerations section for more information).
3. Packages: P: DIP-8C, D: SO-8C.

- V_{MIN} and V_{MAX} [D40] and [D41] show the minimum and maximum DC voltages on the input bulk capacitors. It is calculated by using the AC input parameters [B3], [B4] and the value of C_{IN} [B11]. If a DC input voltage is used, you may enter the values in cells [B40] and [B41]. Entering values in these cells will overwrite the calculated values.
- The transformer's feedback winding turns are shown in cell [D44]. If necessary entering a different number in cell [B44] will change the feedback voltage [D45].
- The feedback resistor values are shown in cells [D46] and [D47]. Enter a value in cell [B46] to change these values. It is not recommended to increase the value greater than 2.5 times the default value. Doing so may activate the open loop protection circuitry.
- If an external bias circuit is desired to reduce no load input power below 200 mW, enter YES in cell [B54]. If not then enter NO.
- If using a bias winding, the recommended bias voltage is shown in cell [D55]. You may change this voltage by entering a value in cell [B55]. It is not recommended to use a value lower than 10 V. Cell [D56] shows the number of turns required for the bias winding. It is important to note that this transformer winding must be AC stacked on top of the feedback winding (placed in series with the feedback winding).
- Enter in cell [B70] the transformer's primary inductance tolerance in percent. The default is 10%.
- Verify that the core's gap L_G [D77], the wire gauge AWG [D82] and the primary's winding current density CMA [D84] are within acceptable limits.
- Use resistor values R_{UPPER} [D46] and R_{LOWER} [D47] for feedback resistors.
- Using PIVS1 [D115] and I_{O1} [D109] determine the proper output rectifier.
- Using V_{MAX} [D41] and I_R [D63] determine the proper input filter capacitors.
- Using V_{O1} [D108] and $I_{RIPPLE1}$ [D114] determine the proper output filter capacitor
- Using I_{AVG} [D61] and the estimated peak reverse voltage, determine the input rectifier diodes. In most cases 1N4007 is ideal.
- Using I_{AVG} [D61] determine the proper input filter inductor current rating.

- If necessary, the output voltage can be fine tuned. After the first prototype is built and running, enter the output voltage in cell [B49] when measured at full load. A fine tuned value for R_{LOWER} [D50] will be calculated to adjust the output voltage.

Step-by-Step Design Procedure

Step 1 – Enter Application Variables VAC_{MIN}, VAC_{MAX}, f_L, V_O, Po, η, Z, t_C, C_{IN}

ENTER APPLICATION VARIABLES					5 V, 6 W Adapter Design
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	5.00			Volts	Output Voltage
PO	6.00			Watts	Output Power
n	0.72				Efficiency Estimate
Z			0.5		Loss Allocation Factor
tC			3	mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	16.80			uFarads	Input Filter Capacitor

Figure 2. Application Variables Section of the Design Spreadsheet.

Determine the input voltage range from Table 3.

Nominal Input Voltage (VAC)	VAC_{MIN}	VAC_{MAX}
100/115	85	132
230	195	265
Universal	85	265

Table 3. Standard Worldwide Input Line Voltage Ranges.

Note: For designs that have a DC rather than an AC input, enter the values for minimum and maximum DC input voltages, V_{MIN} and V_{MAX}, directly into the grey override cell on the design spreadsheet (see Figure 3).

Line Frequency, F_L

50 Hz for universal or single 100 VAC, 60 Hz for single 115 VAC input. 50 Hz for single 230 VAC input. These values represent typical line frequencies rather than minimum. For most applications this gives adequate overall design margin. For absolute worst case or based on the product specification reduce these numbers by 6% (47 Hz or 56 Hz). For half-wave rectification use $F_L/2$. For DC input enter the voltage directly into Cells [B40] and [B41].

Nominal Output voltage, V_O (V)

Enter the nominal output voltage.

Output Power, P_O (W)

Enter the output power.

Power Supply Efficiency, η

Enter the estimated efficiency of the complete power supply measured at the output terminals under full load conditions and worst-case line (generally lowest input voltage). Initial values are provided in table 1. After measuring the efficiency of the first prototype-board at full load and both VAC_{MIN} and VAC_{MAX} if the measured efficiency is different than estimated then enter the measured value and refine the transformer design.

Power Supply Loss Allocation Factor, Z

This factor represents the proportion of losses between the primary and the secondary of the power supply. Z factor is used together with the efficiency number to determine the actual power that must be delivered by the power stage. For example losses in the input stage (EMI filter, rectification etc) are not processed by the power stage (transferred through the transformer). Although they reduce efficiency, the transformer design is not impacted.

$$Z = \frac{\text{Secondary Side Losses}}{\text{Total Losses}}$$

Start with a value of 0.5 if no other data is available.

Bridge Diode Conduction Time, t_C (ms)

This is the duration of the incoming AC sine wave during which the input diodes conduct, charging the input capacitance. This value is used in the calculation of the minimum voltage across the input capacitance at $VAC_{(MIN)}$. The actual value for t_C can be found by measuring the input current waveform on a prototype. Use a value of 3 ms if no other data is available.

Total Input Capacitance, C_{IN} (μF)

Enter total input capacitance using table 4 for guidance.

Total Input Capacitance Per Watt Output Power (μF/W)	
AC Input Voltage (VAC)	Full Wave Rectification
100/115	3
230	1
85-265	3

Table 4. Suggested Total Input Capacitance for Different Input Voltage Ranges.

The capacitance is used to calculate the minimum and maximum DC voltage across the bulk capacitor and should be selected to keep the minimum DC input voltage, V_{MIN} >70 V and D_{MAX} <54%.

DC INPUT VOLTAGE PARAMETERS					
VMIN			96	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

Figure 3. DC Input Voltage Parameters Section of the Design Spreadsheet.

Step 2 – Enter LinkSwitch-CV Variables: LinkSwitch-CV Device, V_{DS} and V_D.

Select a LinkSwitch-CV device based on the input voltage range and output power using Table 2 for guidance.

Reflected Output Voltage, (V_{OR})
This parameter sets the turns ratio between primary and secondary windings. For a given operating condition, a lower V_{OR} will reduce the peak drain voltage, increase the output rectifier's conduction time and reduce the output filter capacitor's ripple current. For a given primary inductance, a lower V_{OR} will reduce the maximum output power. It is recommended to use the default V_{OR} value for the first design iteration.

LinkSwitch-CV On State Drain to Source Voltage, V_{DS} (V)
This parameter is the average ON state voltage developed across the DRAIN and SOURCE pins of LinkSwitch-CV. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

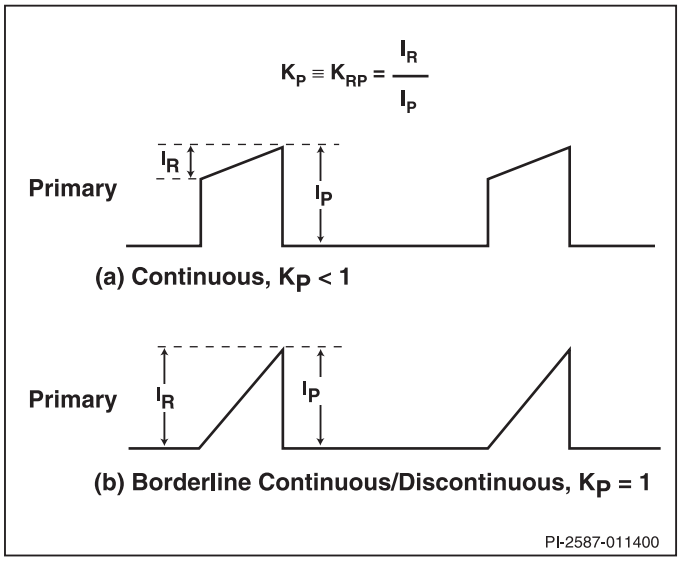


Figure 5. Continuous Conduction Mode Primary Current Waveforms, $K_P \leq 1$.

ENTER LinkSwitch-CV VARIABLES					
LinkSwitch-CV	LNK625P		LNK625P		Chosen LinkSwitch-CV device
ILIMITMIN			0.307	Amps	LinkSwitch-CV Minimum Current Limit
ILIMITMAX			0.353	Amps	LinkSwitch-CV Maximum Current Limit
fS			100000	Hertz	LinkSwitch-CV Switching Frequency
I2FMIN			9801	A^2Hz	LinkSwitch-CV Min I2F (power Coefficient)
I2FMAX			12741	A^2Hz	LinkSwitch-CV Max I2F (power Coefficient)
VOR			90	Volts	Reflected Output Voltage
VDS			10	Volts	LinkSwitch-CV on-state Drain to Source Voltage
VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
DCON			5.04	us	Output Diode conduction time
KP_TRANSIENT			1.04		Worst case ripple to peak current ratio. Maintain KP_TRANSIENT below 0.25

Figure 4. LinkSwitch-CV Parameters Section of Design Spreadsheet.

Output Diode Forward Voltage Drop, V_D (V)
Enter the average forward voltage drop of the (main) output diode. Use 0.5 V for a Schottky diode or 0.7 V for a PN junction diode if no better data is available. By default, a value of 0.5 V is assumed.

Output Diode Conduction Time, D_{CON} (µs)
This is the calculated diode conduction time of the output diode. This value should always be greater than 3.1 µs, the point at which the voltage on the FEEDBACK pin of LinkSwitch-CV is sampled.

Ripple to Peak Drain Current Ratio, $K_{P(TRANSIENT)}$
K_P is the calculated ratio of ripple to peak primary current. $K_{P(TRANSIENT)}$ is the lowest value of K_P that occurs between the first and second switching cycles after a switching cycle has been skipped. This value should be kept above a value of 0.25 to prevent the current limit being triggered after leading edge blanking.

Step 3 – Choose Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, BW, L

These symbols represent core effective cross-sectional area A_E (cm^2), core effective path length L_E (cm), core ungapped effective inductance A_L (nH/Turn^2), bobbin width BW (mm) and number of primary layers L.

By default, if the Core cell is left empty, the spreadsheet selects the smallest core size that meets the peak flux density limit. The user can change this selection and choose an alternate core from a list of commonly available cores (shown in Table 5). Enter the core type from the drop down menu. If the desired core is not listed, then you may enter a core's characteristics A_E, L_E and A_L and the bobbin width BW.

For designs that require safety isolation between primary and secondary but are not using triple insulated wire. The width of the safety margin to be used on each side of the bobbin should be entered for M. Typically for universal input designs a total margin of 6.2 mm would be required, and a value of 3.1 mm would be entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical, however if a total margin of 6.2 mm were required then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin.

For designs using triple insulated wire it may still be necessary to enter a small margin in order to meet the required safety creepage distances. Typically many bobbins exist for each core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required. As the margin reduces the available area for the windings, margin construction may not be suitable for small

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	Auto		**EE16**		Transformer Core size
Core		*EE16*		*P/N:*	PC40EE16-Z
Bobbin		*EE16_BOBBIN*		*P/N:*	BE-16-118CPH
AE			0.192	cm^2	Core Effective Cross Sectional Area
LE			3.5	cm	Core Effective Path Length
AL			1140	nH/T^2	Ungapped Core Effective Inductance
BW			8.5	mm	Bobbin Physical Winding Width
M			0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L			3		Number of Primary Layers
NS			7		Number of Secondary Turns

Figure 6. Transformer Core and Construction Variables Section of the Design Spreadsheet.

Transformer Core Size	
EE10	EF16
EF12.6	EF20
EE13	EF25
EE16	EFD15
EE19	EFD20
EE22	EFD25
EEL16	EFD30
EE16W	EI16
EEL19	EI19
EEL22	EI22
EE25	EI25
EEL25	

Table 5. List of Cores Provided in LinkSwitch-CV PIXls Spreadsheet.

core sizes. If after entering the margin more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design using triple insulated wire.

If your requirements require the use of margin tape, enter the tape width in mm for M.

Enter the number of primary layers (L). The maximum recommended primary layers is 3. Larger number of layers increases leakage inductance which increases losses and degrades output regulation.

N_S is the number of secondary turns. If left blank the lowest number of turns to meet an acceptable core flux density will be calculated.

Step 4 – Feedback Variables

The feedback parameters are calculated by the software. N_{FB} is the number of turns for the feedback winding. The user can change the value by entering the desired number in the shaded cell. V_{FLY} is the flyback voltage on the feedback winding. This voltage is used to regulate the output voltage. Resistors R_{UPPER} and R_{LOWER} are the feedback resistors connected to the feedback winding and the FB pin of the LinkSwitch-CV device. You may enter another value in the shaded cell to change R_{UPPER} and R_{LOWER} will be re-calculated. It is not recommended to increase the value greater than 2.5 times the default value. Doing so may activate the open loop protection circuitry.

After the first prototype is operating, the output voltage can be fine tuned for increased accuracy. Measure the output voltage at full load and enter the value in the Measured Output Voltage cell. R_{LOWER_FINE} will be calculated based on this measured value. Use this value to replace the existing R_{LOWER} in the prototype.

Step 5 – Bias Winding Parameters

If an external bias circuit is desired to reduce no load input power below 200 mW, enter YES in shaded cell. If not, enter NO. If using a bias winding, the recommended bias voltage is shown in cell for V_B. You may change this voltage by entering a value in the shaded cell. It is not recommended to use a value

FEEDBACK VARIABLES					
NFB			6.00		Feedback winding number of turns
VFLY			4.71	Volts	Voltage on the Feedback winding when LinkSwitch-CV turns off
RUPPER			10.00	k-ohms	Upper resistor of feedback network
RLOWER			7.50	k-ohms	Lower resistor of feedback network
Fine Tuning Section					
Measured Output Voltage			5.00	k-ohms	Actual (Measured) Voltage at the output of power supply
RLOWER_FINE			7.50	k-ohms	Adjusted (Fine tuned) value of lower resistor (RLOWER). Do not change value of RUPPER

Figure 7. Feedback Variables Section of the Design Spreadsheet.

Bias Winding Parameters					
Add Bias winding	YES		YES		Enter 'Yes' if you want to add a Bias winding
VB			10	Volts	Bias Winding Voltage
NB			7		Number of Bias winding turns. Bias winding is assumed to be AC stacked on top of the Feedback winding

Figure 8. Bias Winding Parameters Section of the Design Spreadsheet.

lower than 10 V. N_B is the number of turns required for the bias winding. It is important to note that this transformer winding must be AC stacked on top of the feedback winding (placed in series with the feedback winding).

typical A_{LG} value multiplied by $1+(L_{P(TOL)}/100)$. This value is typically used by transformer vendors to purchase the cores with the correct gap size.

CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.51		Maximum Duty Cycle
IAVG			0.09	Amps	Average Primary Current
IP			0.31	Amps	Minimum Peak Primary Current
IR			0.27	Amps	Primary Ripple Current
IRMS			0.13	Amps	Primary RMS Current

Figure 9. Current Waveform Shape Parameters Section of the Design Spreadsheet.

Step 6 – Iterate Transformer Design and Generate Key Transformer Design Parameters

Iterate the design, making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column. Messages marked "!!! Info" provide guidance for acceptable parameters that can be further optimized. Once all warnings have been cleared, use the transformer design parameters to either wind a prototype transformer, or to send to a vendor for obtaining samples.

Maximum Flux Density, B_M (Gauss)

B_M is the operating core flux density. A maximum value of 2500 (0.25 T) is recommended to minimize audible noise generation. Values above this will depend on acceptability of audible noise levels. If using long cores, for example EEL16, the flux density may need to be reduced even further to give acceptable levels.

Peak Flux Density, B_P (Gauss)

B_P is the maximum flux density at maximum device current limit and inductance tolerance. To prevent core saturation a maximum value of 3100 Gauss (0.31 T) is recommend.

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LPMIN			1479	uHenries	Minimum Primary Inductance
LP TYP			1627	uHenries	Typical (Nominal) Primary Inductance
LP TOL			10		Tolerance of Primary inductance
NP			115		Primary Winding Number of Turns
ALG			124	nH/T^2	Gapped Core Effective Inductance
BM			2441	Gauss	Maximum Flux Density, (BM<2500) Calculated at typical current limit and typical primary inductance
BP			2848	Gauss	Peak Flux Density, (BP<3100) Calculated at maximum current limit and maximum primary inductance
BAC			950	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1654		Relative Permeability of Ungapped Core
LG			0.19	mm	Gap Length (Lg > 0.1 mm)
BWE			25.5	mm	Effective Bobbin Width
OD			0.22	mm	Maximum Primary Wire Diameter including insulation
INS			0.04	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.18	mm	Bare conductor diameter
AWG			34	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			40	Cmils	Bare conductor effective area in circular mils
CMA			301	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

Figure 10. Transformer Primary Design Parameters Section of the Design Spreadsheet.

Primary Inductance, $L_{P(TYP)}$, $L_{P(MIN)}$ (mH), $L_{P(TOLERANCE)}$, (%)

$L_{P(MIN)}$ represents the minimum primary inductance needed to deliver the nominal output power (P_O).

As it is more common to specify the primary inductance to a vendor as a nominal value with tolerance, the value for $L_{P(TYP)}$ is calculated via the expression

$$L_{P(TYP)} = L_{P(MIN)} \times \left(1 + \frac{L_{P(TOL)}}{100}\right)$$

where $L_{P(TOL)}$ is the entered percentage tolerance. If no value is entered, PIXls uses 10 by default, signifying $L_{P(TOL)}$ of ±10%.

Primary Winding Number of Turns, N_P

This is the total number of primary winding turns.

Gapped Core Effective Inductance, A_{LG} (nH/T^2)

This is the target core effective inductance at $L_{P(MIN)}$ for the

Core Gap Length, L_G (mm)

L_G is the estimated core gap length. Values below 0.1 mm are generally not recommended for center-leg gapped cores due to the resultant increase in primary inductance tolerance. If you require such a low value, consult with your transformer vendor for guidance.

Maximum Primary Winding Wire Outside Diameter, OD (mm)

This is the calculated maximum outside wire diameter to allow the primary winding to fit into the number of specified layers. When selecting the wire type use double-coated magnetic wire (rather than single-coated types) for improved reliability and reduced primary capacitance (lower no-load input power).

Primary Winding Wire Bare Conductor Diameter, DIA (mm)

Primary Winding Wire Gauge, AWG

This is the calculated conductor diameter rounded to the next smallest standard American Wire Gauge size.

Primary Winding Bare Conductor Effective Area, CM(C_{MILS})
CM is the effective conductor area in circular mils.

Primary Winding Wire Current Capacity, CMA (C_{MILS}/A)
CMA is the primary conductor area in circular mils (where 1 mil = 1/1000th of an inch) per Amp. Values below the recommended minimum of 200 maybe acceptable if worst case winding temperature is verified.

Step 7 – Selection of Input Stage

The recommended input stage is shown in Table 6. It consists of a fusible element, input rectification, and line filter network. The fusible element can be either a fusible resistor or a fuse. If a fusible resistor is selected, use a flameproof type. Depending on the differential line input surge requirements, a wire-wound type may be required. Avoid using metal or carbon film types as these can fail due to the inrush current when VAC_{MAX} is applied repeatedly to the supply.

For designs using a Y-capacitor and a single inductor or inductor plus ferrite bead the inductor should be located on the opposite side to the Y-capacitor connection. For example with the Y-capacitor connected to positive of C_{IN2} the inductor should be in the location of L_{IN2} and ferrite bead L_{IN1} (if used).

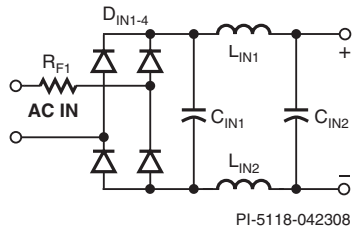
For designs with outputs ≤1 W, it is generally lower cost to use half-wave rectification; and >1 W, full-wave rectification. The EMI immunity of half-wave rectified designs is improved by adding a second diode in the lower return rail. This provides EMI gating (EMI currents only flow when the diode is conducting) and doubles the differential surge immunity since the surge voltage is shared across two diodes.

Half-wave rectification may be unsuitable if the supply specification requires output electrostatic discharge (ESD) testing. During such testing up to ±15 kV discharges of fixed energy are applied to the secondary of the supply (with respect to the primary). With half-wave rectification this voltage also appears across the input diodes, and may cause failure. With full-wave rectification the diode stress is clamped to the voltage across the input capacitance, preventing diode failure.

Conducted EMI filtering is provided by L_{IN1} and L_{IN2}, which together with C_{IN1} and C_{IN2}, form a pi (π) filter. A single inductor is suitable for designs below 3 W or when EMI is measured with the output of the supply floating (i.e. not connected to safety earth ground). Although two inductors are generally required above 3 W, a ferrite bead may be sufficient, especially when the output of the supply is floating.

Normally the total input capacitance is divided equally between the two input capacitors (C_{IN1} and C_{IN2}). However, for lower cost, two different capacitance values may be used. In this case select C_{IN1} as ≥1 μF (or as needed) to prevent overvoltage of the capacitor during differential mode surge. Select the second capacitor C_{IN2} to meet both an overall capacitance (C_{IN1} + C_{IN2}) of ≥2 μF/W of output power, and 3 μF/W of output power for highest low-line efficiency.

Differential-mode EMI generation is a strong function of the equivalent series resistance (ESR) of C_{IN2}, as this capacitor supplies the primary switching current. Selecting a lower ESR capacitor series for C_{IN2} than C_{IN1} can help reduce differential mode (low frequency) conducted EMI while optimizing the overall cost of the two capacitors. Table 6 shows the input filter schematic, gives a formula for selecting C_{IN1} + C_{IN2}, and tells how to adjust the input capacitance for other input voltage ranges.



R_{F1}: 4.7 Ω – 10 Ω, 1 W, Fusible, flameproof or fuse
L_{IN1}: 470 μH – 2.2 mH, 0.05 A – 0.3 A
L_{IN2}: Ferrite bead or 470 μH – 2.2 mH, 0.05 A – 0.3 A
C_{IN1} + C_{IN2}: ≥ 2 μF/W_{OUT}, 400 V, 85 VAC - 265 VAC
: ≥ 2 μF/W_{OUT}, 200 V, 100 VAC - 115 VAC
: ≥ 1 μF/W_{OUT}, 400 V, 185 VAC - 265 VAC
D_{INX}: 1N4007, 1 A, 1000 V

Table 6. Input Stage Recommendation

Step 8 – Selection of BYPASS Pin Capacitor, Bias Winding and Feedback Components

BYPASS Pin Capacitor
Use a 1 μF BYPASS pin capacitor (C4 in Figure 1) with a voltage rating greater than 7 V. The capacitor's dielectric material is not critical. However, the absolute minimum value (including tolerance and temperature) should be ≥0.5 μF. The capacitor must be physically located close to the LinkSwitch-CV BYPASS pin.

Bias Winding Components
The addition of a bias circuit decreases the no-load input power from ~200 mW down to less than 70 mW. This may sufficiently increase efficiencies at lighter loads to allow lower cost components while still meeting average efficiency requirements. For example a PN-junction diode may replace a higher-cost Schottky-barrier diode, or the output cable may be replaced by one constructed of smaller diameter wire (higher impedance).

The power supply schematic shown in Figure 1 uses the bias circuit. Diode D6, capacitor C6, and resistor R4 form the bias circuit. If the output voltage is less than 10 V, then an additional transformer winding is needed, AC-stacked on top of the feedback winding. This provides a high enough voltage to supply the BYPASS pin even during low switching frequency operation at no-load.

In Figure 1 the additional bias winding (from pin 5 to pin 4) is stacked on top of the feedback winding (pin 4 to pin 2). Diode D6 rectifies the output and C6 is the filter capacitor. A 10 μF capacitor is recommended to hold up the bias voltage during

the low frequency operation at no-load. The capacitor type is not critical but its voltage rating should be above the maximum value of V_{BIAS}. The recommended current into the BYPASS pin is equal to the IC supply current (~0.5 mA). The value of R_{BIAS} (R4) is calculated according to

$$R_{BIAS} = (V_{BIAS} - V_{BP})/I_{S2}$$

where V_{BIAS} (10 V typical) is the voltage across C6, I_{S2} (0.5 mA typical) is the IC supply current, and V_{BP} (6.0 V typical) is the BP pin voltage. The parameters I_{S2} and V_{BP} are provided in the parameter table of the LinkSwitch-CV data sheet. Diode D6 can be any low-cost diode such as FR102, 1N4148, or BAV19/20/21. The diode voltage stress is given in the Voltage Stress Parameter section of the design spreadsheet.

If the feedback winding voltage (V_{FLY} in the design spreadsheet) is >10 V an additional winding is not required. In this case, connect D6 directly to the feedback winding at pin 4 of the transformer and eliminate the bias winding between pins 5 and 4.

Feedback Pin Resistor Values

The values of R_{UPPER} and R_{LOWER} can be found in cells [D46] and [D47] for the initial prototype build. In applications where a different feedback network impedance is required, a value can be entered for R_{UPPER}, the software will calculate the value of R_{LOWER}. It is important to note that the FEEDBACK pin requires a minimum of 150 μA of input current to detect that the feedback network is present. If the current is less than 150 μA, the power supply may not start properly. Resistors R_{UPPER} and R_{LOWER} should be located as close to the FEEDBACK pin as possible. After the first prototype is running, it may be necessary to adjust the output voltage by adjusting the value of R_{LOWER}. PIXls will calculate the proper value. Enter the measured output voltage in cell [B49] and PIXls will display the new value for R_{LOWER} in cell [D50].

Capacitor C5 and R5 in figure 1 are used to eliminate the effects of pulse grouping. Please see the section on pulse grouping in the Tips for Designs section for more information.

Step 9 – Selection of Output Diode and Pre-load Output Rectifier Diode

The output rectifier diode should be either a fast or an ultrafast recovery PN junction or Schottky-barrier type. Select a diode with sufficient margin to the specified voltage rating (V_R). Typically $V_R \geq 1.2 \times$ PIVs, where PIVs is taken from the Voltage Stress Parameters section of the spreadsheet. Once a prototype is completed use an oscilloscope to measure the actual diode stress at VAC_{MAX} to confirm acceptable de-rating (typically 80%).

Select the diode with the closest rating to $I_D \geq 2 \times I_O$, where I_D is the diode's rated current and I_O is the output current. Take the diode's self-heating into consideration and use a larger diode, if needed, to meet thermal or efficiency requirements.

Table 7 lists some of the suitable Schottky and ultrafast diodes that may be used with LinkSwitch-CV circuits. As the output voltage is sampled at the switching frequency, a minimum switching frequency is maintained at no-load to give acceptable transient load performance. Therefore, if the supply can operate unloaded, use a pre-load resistor to prevent the output voltage from rising under very light (<~25 mA) or no-load conditions (see resistor R7, R8 and R9 in Figure 1).

For designs where output voltage regulation must be maintained at zero load, start with a resistor value that represents a load of approximately 25 mA at the nomimal output voltage. For example, for a 5 V output use a pre-load resistor value of 2 kΩ.

For designs where the output voltage can rise under no-load conditions, select the pre-load resistor value such that the output voltage is within the maximum output voltage specification. Limit the maximum voltage rise at no-load to <50% of the normal output voltage to minimize increases in input power due to increases in the primary clamp and bias winding dissipation.

Since a pre-load resistor also increases the no-load losses, where the specification allows, adjust the no-load voltage to trade-off lower no-load input power with high no-load output voltage as needed.

Series Number	Type	VR Range	I_F	Package	Manufacturer
		V	A		
1N5817 to 1N5819	Schottky	20-40	1	Leaded	Vishay
SB120 to SB1100	Schottky	20-100	1	Leaded	Vishay
11DQ50 to 11DQ60	Schottky	50-60	1	Leaded	Vishay
1N5820 to 1N5822	Schottky	20-40	3	Leaded	Vishay
MBR320 to MBR360	Schottky	20-60	3	Leaded	Vishay
SS12 to SS16	Schottky	20-60	1	SMD	Vishay
SS32 to SS36	Schottky	20-60	3	SMD	Vishay
UF4002 to UF4006	Ultrafast	100-600	1	Leaded	Vishay
UF5401 to UF5408	Ultrafast	100-800	3	Leaded	Vishay
ES1A to ES1D	Ultrafast	50-200	1	SMD	Vishay
ES2A to ES2D	Ultrafast	50-200	2	SMD	Vishay
SL12 to SL23	Schottky (low V_F)	20-30	1	SMD	Vishay
SL22 to SL23	Schottky (low V_F)	20-30	2	SMD	Vishay
SL42 to SL44	Schottky (low V_F)	20-30	4	SMD	Vishay

Table 7. List of Suitable Diodes for LinkSwitch-CV Designs.

TRANSFORMER SECONDARY DESIGN PARAMETERS					
Lumped parameters					
ISP			5.02	Amps	Peak Secondary Current
ISRMS			2.14	Amps	Secondary RMS Current
IO			1.20	Amps	Power Supply Output Current
IRIPPLE			1.78	Amps	Output Capacitor RMS Ripple Current
CMS			429	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			23	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.58	mm	Secondary Minimum Bare Conductor Diameter
ODS			1.21	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			0.32	mm	Maximum Secondary Insulation Wall Thickness

Figure 11. Transformer Secondary Design Parameters Section of Design Spreadsheet.

VOLTAGE STRESS PARAMETERS					
VDRAIN			584	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVB			48	Volts	Bias Diode Maximum Peak Inverse Voltage
PIVS			28	Volts	Output Rectifier Maximum Peak Inverse Voltage

Figure 12. Voltage Stress Parameters Section of Design Spreadsheet.

Step 10 – Select Output Filter Capacitor

Select the capacitor voltage to be ≥1.2 × $V_{O(MAX)}$.

Select the initial capacitor choice using the maximum allowable equivalent series resistance (ESR) expression below:

$$ESR_{MAX} = \frac{V_{RIPPLE(MAX)}}{I_{SP}}$$

Where $V_{RIPPLE(MAX)}$ is the maximum specified output ripple and noise and ISP is the secondary peak current from the Transformer Secondary Parameters section of the design spreadsheet.

The absolute minimum capacitance (excluding the effect of ESR) is given by:

$$C_{OUT(MIN)} = \frac{I_{O(MAX)}\left(\frac{1}{F_S} - D_{CON}\right)}{V_{RIPPLE(MAX)}}$$

Where $I_{O(MAX)}$ is the maximum output current, F_S is switching frequency, D_{CON} is the output diode conduction time and $V_{RIPPLE(MAX)}$ is the maximum allowable output ripple voltage. Verify that the ripple current rating of the capacitor is above the I_{RIPPLE} value (from the Transformer Secondary Parameters section of the design spreadsheet). If not, select the smallest capacitance value that meets this requirement. Many capacitor manufacturers provide factors that increase the ripple current rating as the capacitor operating temperature is reduced from the data sheet maximum. This should be considered to ensure that the capacitor is not oversized for cost reasons.

To reduce the physical size of the output capacitor an output LC post filter can be used to reduce the ESR related switching noise. In this case select either a 1 μH to 3.3 μH inductor with a current rating ≥I_O or a ferrite bead for designs with I_O<~500 mA. The second capacitor is typically 100 μF or 220 μF with a low ESR for good transient response. As the secondary ripple current does not pass through this capacitor there are no specific ESR or ripple current requirements.

TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)					
1st output					
VO1			5	Volts	Output Voltage (if unused, defaults to single output design)
IO1			1.200	Amps	Output DC Current
PO1			6.00	Watts	Output Power
VD1			0.5	Volts	Output Diode Forward Voltage Drop
NS1			7.00		Output Winding Number of Turns
ISRMS1			2.14	Amps	Output Winding RMS Current
IRIPPLE1			1.78	Amps	Output Capacitor RMS Ripple Current
PIVS1			28	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS1			429	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS1			23	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS1			0.58	mm	Minimum Bare Conductor Diameter
ODS1			1.21	mm	Maximum Outside Diameter for Triple Insulated Wire
2nd output					
VO2				Volts	Output Voltage
IO2				Amps	Output DC Current
PO2			0.00	Watts	Output Power
VD2			0.7	Volts	Output Diode Forward Voltage Drop
NS2			0.89		Output Winding Number of Turns
ISRMS2			0.00	Amps	Output Winding RMS Current
IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS2			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS2			N/A	mm	Minimum Bare Conductor Diameter
ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
3rd output					
VO3				Volts	Output Voltage
IO3				Amps	Output DC Current
PO3			0.00	Watts	Output Power
VD3			0.7	Volts	Output Diode Forward Voltage Drop
NS3			0.89		Output Winding Number of Turns
ISRMS3			0.00	Amps	Output Winding RMS Current
IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
PIVS3			3	Volts	Output Rectifier Maximum Peak Inverse Voltage
CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
DIAS3			N/A	mm	Minimum Bare Conductor Diameter
ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
Total power			6	Watts	Total Output Power
Negative Output			N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

Figure 13. Transformer Secondary Design Parameters for Multiple Outputs Section of Design Spreadsheet.

The output capacitor may also be split into two physical capacitors. Here the overall ripple current rating is equal to the sum of the ratings of each individual capacitor.

Step 11 – Selection of Primary Clamp Components

Two clamp arrangements, shown in Figure 14, are suitable for LinkSwitch-CV designs. Minimize the value of C_{C1} and maximize R_{C2} while maintaining the peak drain voltage to <680 V. Larger values of C_{C1} may cause higher output ripple voltages due to the longer settling time of the clamp voltage impacting the sampled voltage on the feedback winding.

The RCDZ circuit is preferred when the primary leakage inductance is greater than 125 μH to reduce drain voltage overshoot and/or ringing present on the feedback winding.

For best output regulation, the feedback voltage must settle to within 1% at 2.1 μs from the turn off of the primary MOSFET. This requires careful selection of the clamp circuit components. The voltage of VR1 is selected to be 10% to 20% above the V_{OR}. This allows the clamp to limit the magnitude of the leakage voltage spike at turn off but ensures the Zener is not conducting during the flyback period when the output diode is conducting. The value of R_{C2} should be the largest value that result in both acceptable settling of the feedback pin voltage and peak drain voltage. Making R_{C2} too large will increase the discharge time of C_{C1}, increase the peak drain voltage and degrade regulation.

Resistor R_{C1} dampens high frequency leakage inductance ringing for reduced EMI. The value must be large enough to dampen the ring in the required time but must not be too large to cause the drain voltage to exceed 680 V.

If the primary leakage inductance is less than 125 μH, VR1 can be eliminated and the value of R_{C2} increased. A value of 470 kΩ with an 820 pF capacitor is a recommended starting point. Verify that the peak drain voltage is less than 680 V under all line and load conditions. Verify the feedback winding settles to an acceptable limit for good line and load regulation.

Effects of Fast vs. Slow Diodes in Clamp Circuit

A slow reverse recovery diode (>1 μs) reduces the feedback voltage ringing and improve output regulation. Using a fast diode (500 ns) increases the amplitude of ringing which can result in increased output ripple. In Figure 15 the (larger) ring amplitude when using a FR104 diode represents up to an 8% error in the sampled voltage over the time period 2.5 μs to 3.1 μs.

Clampless Designs

Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore the maximum AC input line voltage, the value of V_{OR}, the leakage inductance energy, (a function of leakage inductance and peak primary current), and the primary winding capacitance determine the peak drain voltage. With no

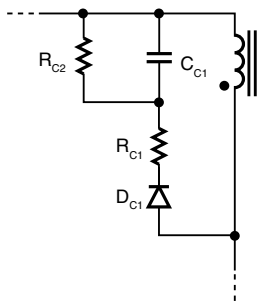
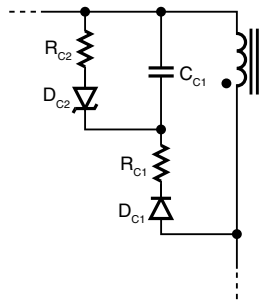
Common Primary Clamp Configurations	
RCD	**RCDZ (Zener Bleed)**
	
D_{C1}: 1N4007 / FR107, 1 A, 1000 V R_{C1}: 100 Ω - 300 Ω, 1/4 W C_{C1}: 470 pF - 1000 pF R_{C2}: 330 kΩ - 680 kΩ, 1/2 W	D_{C1}: 1N4007 / FR107, 1 A, 1000 V D_{C2}: BZY97Cxxx (xxx = 1.1 to 1.2 × V_{OR}) R_{C1}: 100 Ω - 300 Ω, 1/4 W R_{C2}: 5 kΩ - 100 kΩ, 1/2 W C_{C1}: 470 pF - 1000 pF

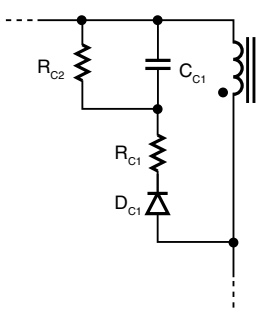
Figure 14. Primary Clamp Configurations Suitable for LinkSwitch-CV Designs.

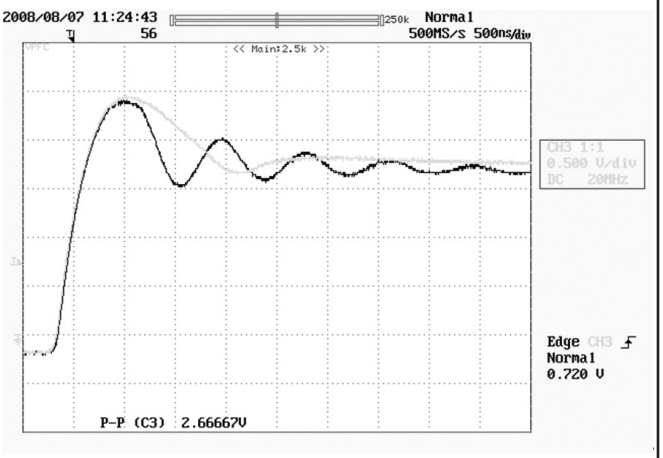
significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only Clampless design:

1. Clampless designs should only be used for P_O ≤5 W using a V_{OR} of ≤90 V
2. For designs with P_O ≤5 W, a two-layer primary must be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF. A bias winding must be added to the transformer using a standard recovery rectifier diode (1N4003 – 1N4007) to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
3. For designs with P_O >5 W, clampless designs are not practical and an external clamp should be used.
4. Ensure that worst-case, high line, peak drain voltage is below the BV_{DSS} specification of the internal MOSFET and ideally ≤650 V to allow margin for design variation. The capacitance of the transformer is much more critical in a clampless design. Therefore ensure that testing is performed with transformers at the minimum of the capacitance (or resonant frequency) specification.

V_{OR} (Reflected Output Voltage), is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The V_{OR} adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.





Black Trace: D_{C1} is a FR104
Gray Trace: D_{C1} is a 1N4007G

Figure 15. Effect of Clamp Diode Recovery Time of Feedback Pin Voltage.

Example Transformer Winding Arrangement Including E-Shields™

Once the PIXls spreadsheet design is complete all the necessary information is available to create a transformer design. In this section some practical tips are presented on winding order and the inclusion of Power Integrations proprietary E-Shield techniques. Shield windings improve conducted EMI performance and simplify the input filter stage by eliminating the need for a common mode choke and reducing the value of or eliminating the Y-class capacitor connected between the primary and secondary. Refer to Figures 16 and 17 to reference winding numbers (WDx).

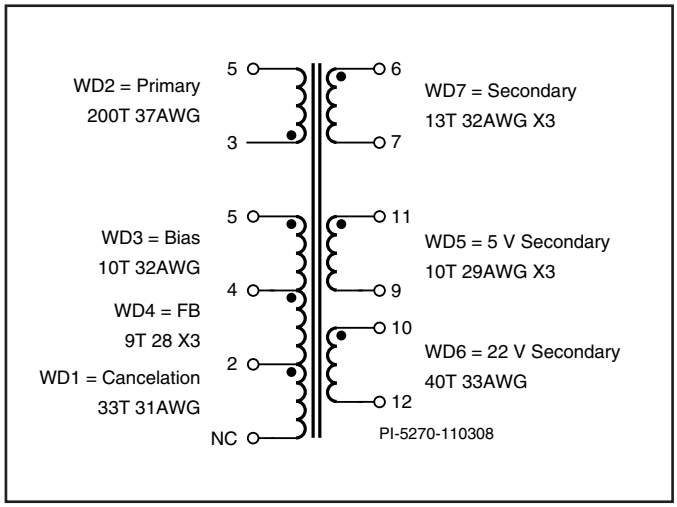


Figure 16. Typical Transformer Electrical Schematic.

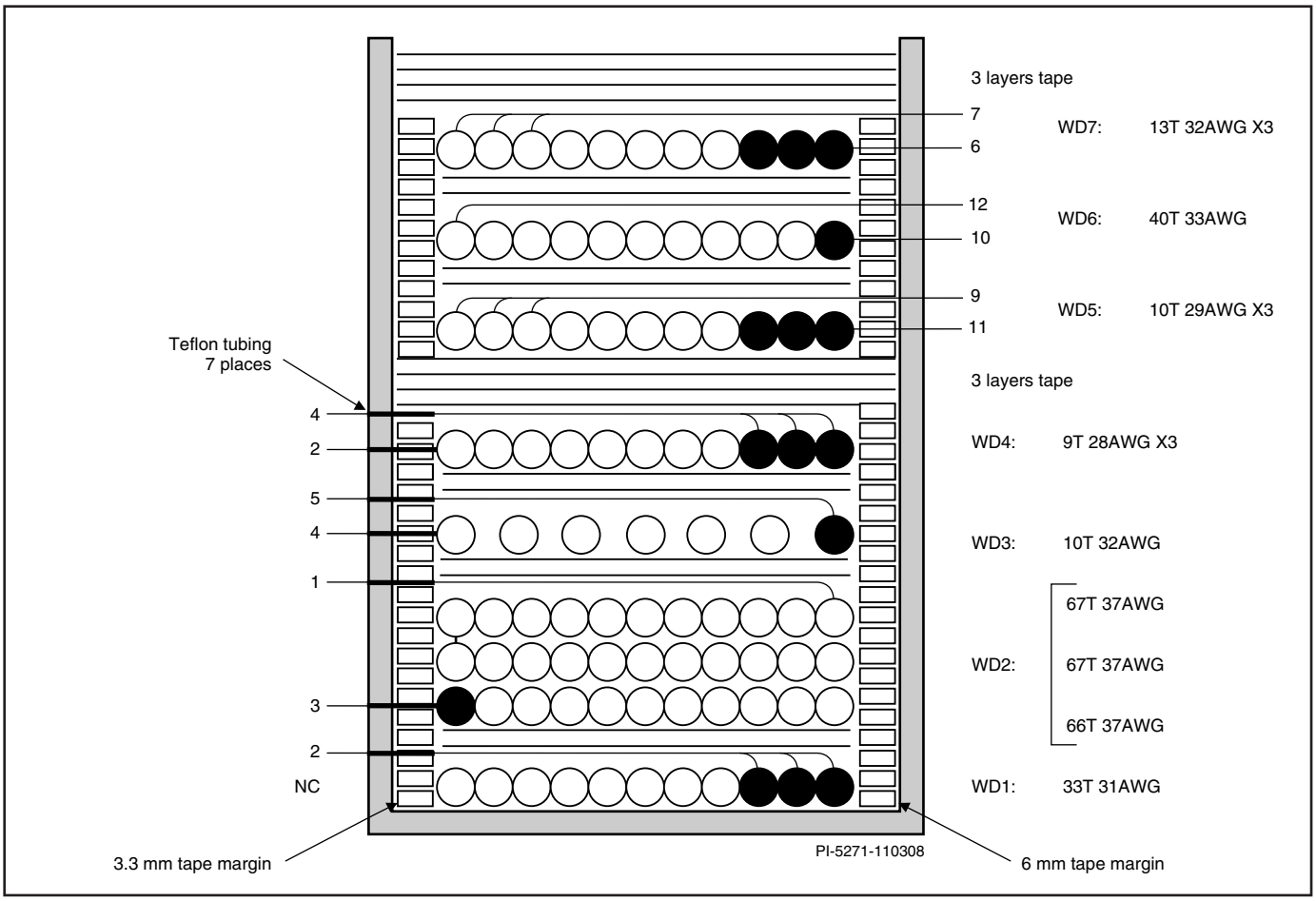


Figure 17. Typical Mechanical Construction of LinkSwitch-CV Transformer.

Core Cancelation Winding

The first layer is the Core Cancelation winding (WD1). The number of turns can be found by taking the primary turns N_P [D71] from PIXls and divide by the number of layers L [E36]. Divide the result by 2 (N_{SHEILD} = 1/2 *(N_P/L)). This gives a starting value and may need to be adjusted to optimize the conducted EMI emissions. Note that the start (black dot) of the Shield winding is on the opposite side of the bobbin from the start of the primary winding. The finish end of the Shield winding is floating. Use a gauge wire that will completely fill the bobbin width.

Primary Winding

The second winding (WD2) is the primary. From PIXls find the number of turns N_P [D71], number of layers L [E36] and the wire gauge AWG [D82]. As shown in figure 17, the start of the primary is on the opposite side of the bobbin from the Shield's start.

Bias Winding (optional)

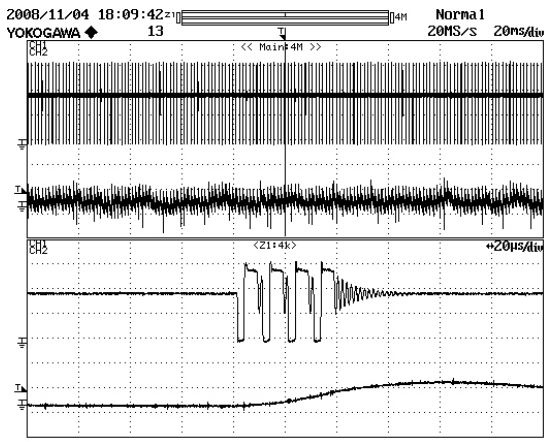
The bias winding is the third winding (WD3). This winding is spread evenly across the bobbin width. Since this winding does not provide shielding, it is not required to fill the layer without gaps. The number of turns N_B are calculated in cell [D56].

Feedback Winding

The feedback winding is the fourth winding (WD4) on the bobbin. From PIXls find the number of turns N_{FB} [D44]. To help reduce conducted EMI emissions, this winding must cover the complete bobbin width. Usually a multi-filiar winding is used to completely cover the bobbin width.

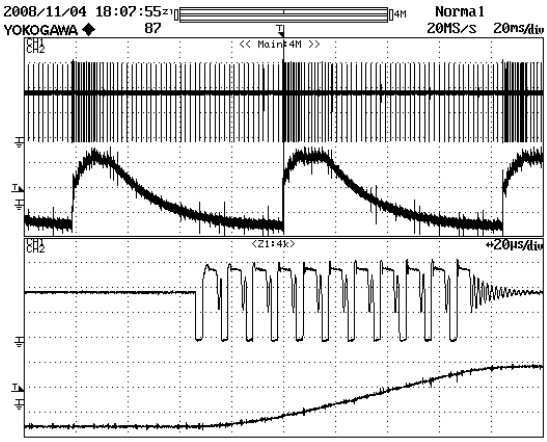
Secondary Winding

The secondary windings begin on layer 5. The main output (highest output power) should be placed on this layer. This layer should fill the bobbin width.



Split Screen with Bottom Portion Zoom of Upper Trigger Point
Top Trace: Drain Waveform (200 V/div)
Bottom Trace: Output Ripple Voltage (50 mV/div)

Figure 18. Not Pulse Grouping (<5 Consecutive Switching Cycles).



Split Screen with Bottom Portion Zoom of Upper Trigger Point
Top Trace: Drain Waveform (200 V/div)
Bottom Trace: Output Ripple Voltage (50 mV/div)

Pulse Grouping (>5 Consecutive Switching Cycles).

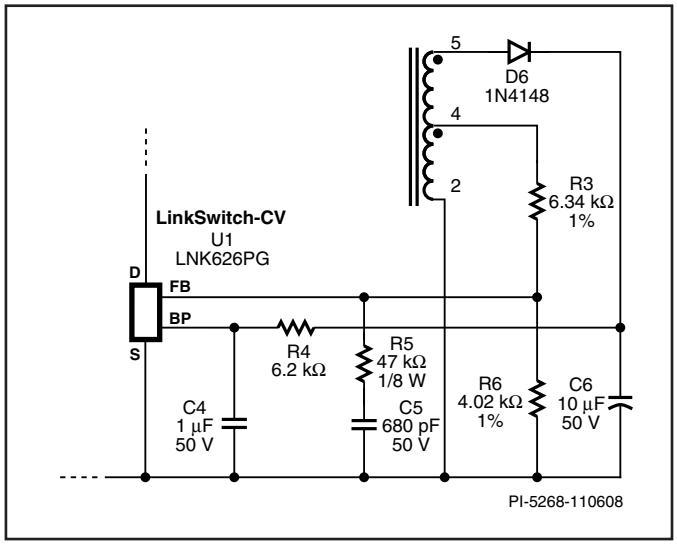


Figure 19. RC Network Across R_{BOTTOM} to Reduce Pulse Grouping.

Additional Secondary Windings
Any additional output windings are added after the main output winding.

Tips for Designs

Pulse Grouping
Pulse grouping is defined as 6 or more consecutive pulses followed by two or more timing state changes. The effect of pulse grouping is increased output voltage ripple. This is shown on the right of Figure 18 where pulse grouping has caused an increase in the output ripple.

To eliminate group pulsing verify that the feedback signal settles within 2.1 μs from the turn off of the internal MOSFET. A Zener diode in the clamp circuit may be needed to achieve the desired settling time. If the settling time is unsatisfactory, then a RC network across R_{LOWER} (R6) of the feedback resistor is necessary.

The value of R (R5 in Figure 19) should be an order of magnitude greater than R_{LOWER} and selected such that R×C = 32 μs where C is C5 in Figure 19 .

Design Recommendations

Circuit Board Layout
LinkSwitch-CV is a highly integrated power supply solution that integrates on a single die, both, the controller and the high voltage MOSFET. The presence of high switching currents and voltages together with analog signals makes it especially important to follow good PCB design practice to ensure stable and trouble free operation of the power supply.

When designing a board for the LinkSwitch-CV based power supply, it is important to follow the following guidelines:

Primary-Side Connections
- Use a single point (Kelvin) connection at the negative terminal of the input filter capacitor for the LinkSwitch-CV SOURCE pin and bias winding return. This improves surge capabilities by returning surge currents from the bias winding directly to the input filter capacitor.
- The BYPASS pin capacitor should be located as close as possible to the SOURCE and BYPASS pins.
- The copper area connected to the source pins provide the LinkSwitch-CV heat sink. A rule of thumb estimate is that the LinkSwitch-CV will dissipate 10% of the output power. Provide enough copper area to keep the source pin temperature below 110 °C.

Secondary
- To minimize leakage inductance and EMI the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminal of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

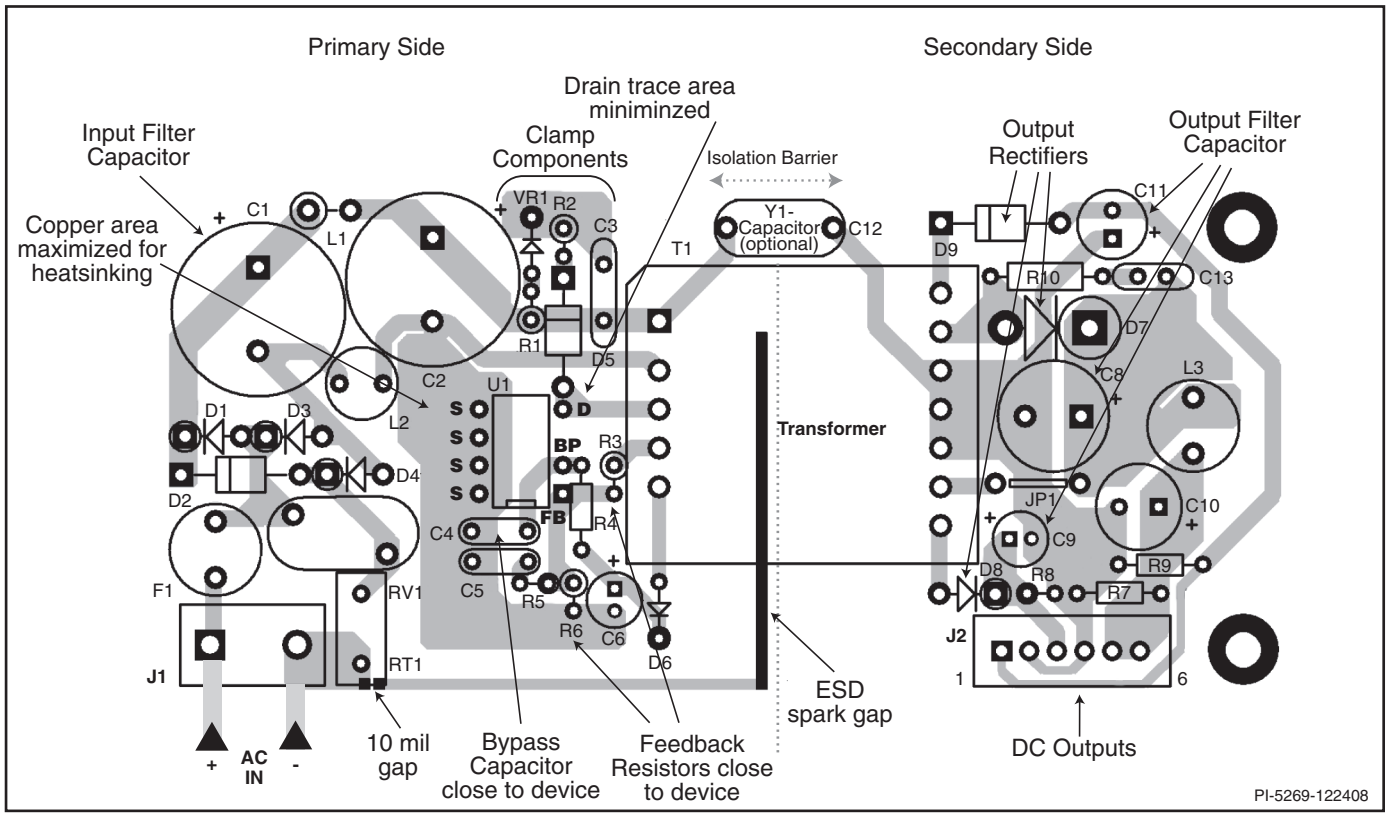


Figure 20. PCB Layout Example of a Three Output Power Supply.

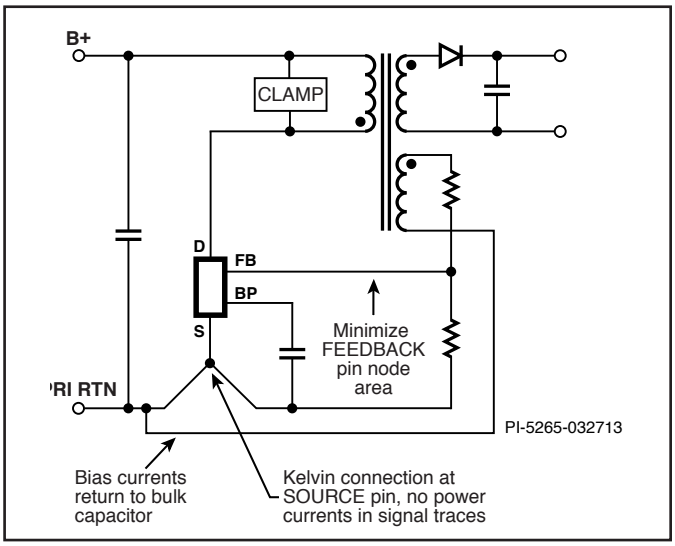


Figure 21. Schematic Representation of Recommended Layout without External Bias.

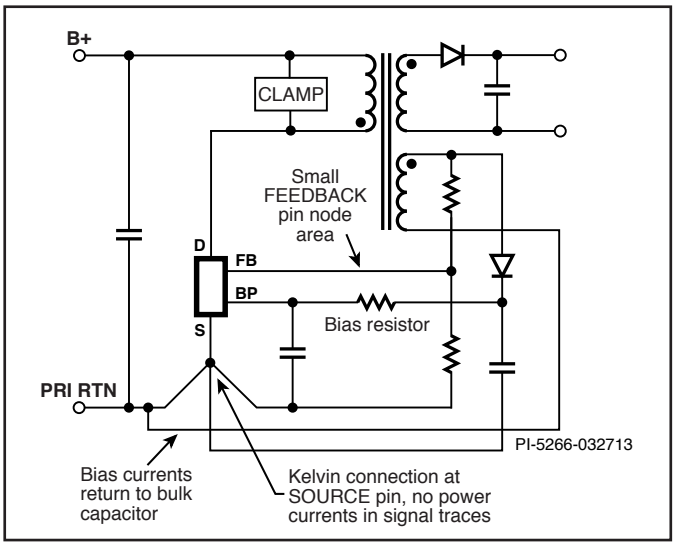


Figure 22. Schematic Representation of Recommended Layout with External Bias.

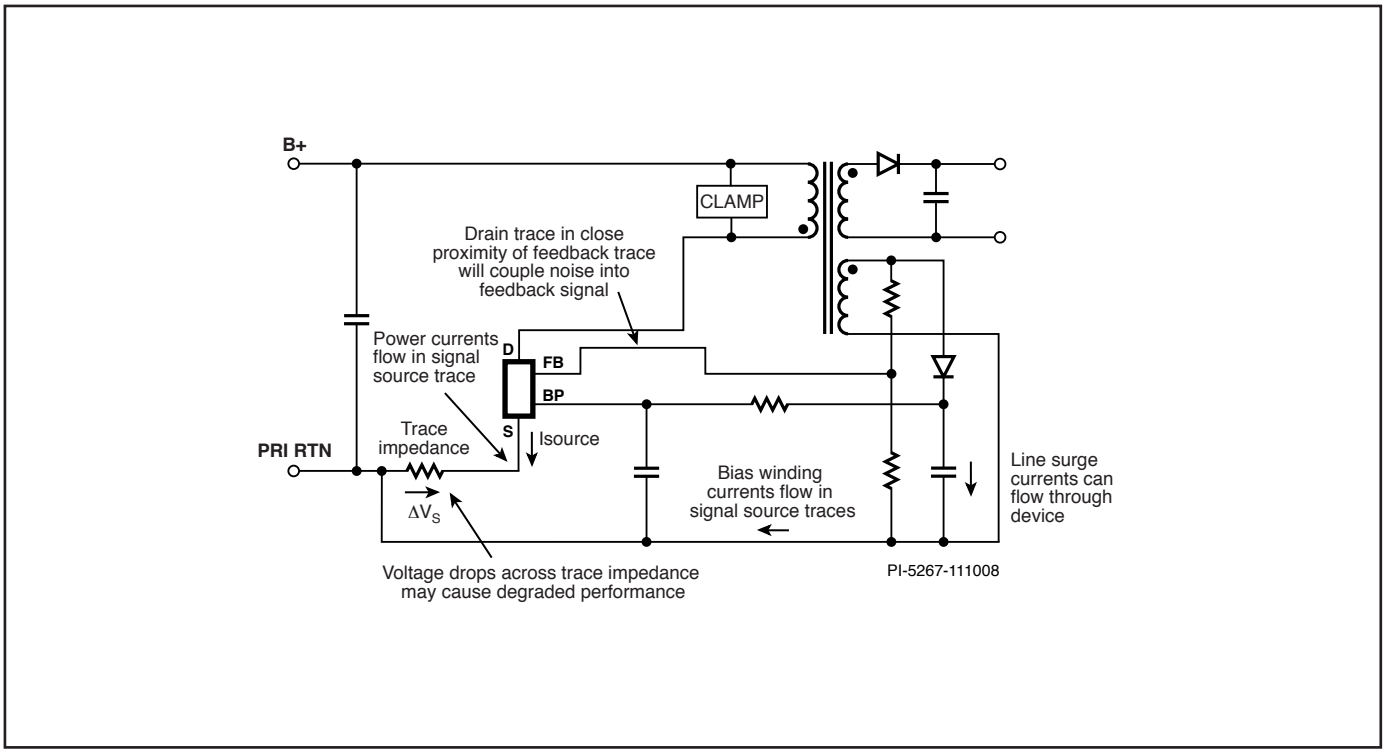


Figure 23. Schematic Representation of Electrical Impact Due to Improper Layout.

- A spark gap is formed by a PCB trace placed under the transformer along the isolation barrier between primary and secondary sides of the layout. During ESD testing any arcing across the isolation barrier will preferentially occur between this trace and the secondary. This safely directs the arc discharge current to the AC input. A small additional gap is placed in this trace near the AC input. The gap electrically isolates the primary side connected trace from the AC and prevents any noise coupling into the AC input but forms a second low breakdown voltage spark gap during ESD testing.

Drain Clamp

LinkSwitch-CV senses the feedback winding on the primary side to regulate the output. It is important to note that the leakage inductance ring can affect the output regulation. A proper drain clamp is needed to eliminate the high frequency ring. Figure 24 shows the desired waveform. Notice in Figure 25 the negative excursion due to the leakage inductance ring. This spike will reduce the output voltage regulation performance and can be improved by adjusting the damping resistor in series with the clamp diode (R_{C1} in Figure 14).

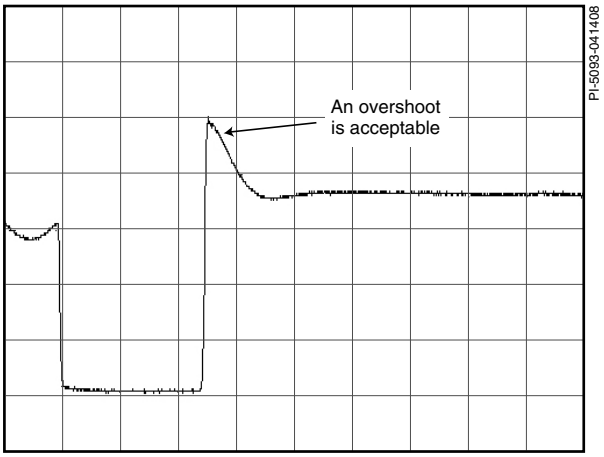


Figure 24. Desired Drain Waveform.

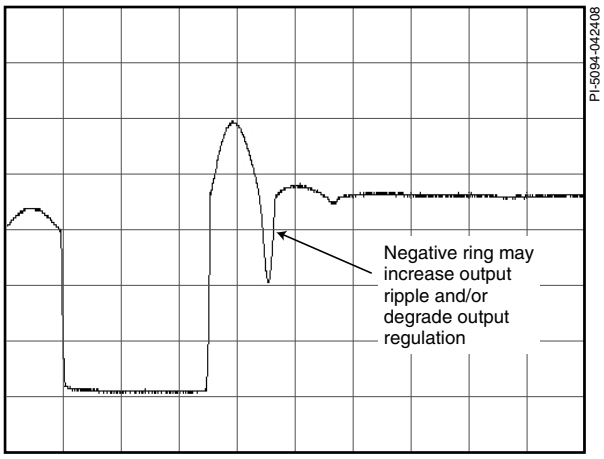


Figure 25. Undesirable Drain Waveform.

Quick Design Checklist

As with any power supply design, all LinkSwitch-CV designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that peak V_{DS} does not exceed 680 V at highest input voltage and maximum output power.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and maximum output load, verify drain current waveforms at start-up for any signs of transformer saturation and excessive leading edge current spikes. LinkSwitch-CV has a leading edge blanking time of 170 ns to prevent premature termination of the ON-cycle. Verify that the leading edge current spike is below the allowed current limit envelope for the drain current waveform at the end of the 170 ns blanking period.
3. Thermal check – At maximum output power, both minimum and maximum input voltage and maximum ambient temperature; verify that temperature specifications are not exceeded for LinkSwitch-CV, transformer, output diodes and output capacitors. Enough thermal margin should be allowed for the part-to-part variation of the $R_{DS(ON)}$ of LinkSwitch-CV, as specified in the data sheet. The maximum source pin temperature is 110 °C.

Notes

Revision	Notes	Date
A	Initial Release.	11/08
B	Revised Figure 20.	01/09
B	Updated Figures 21 and 22.	03/27/13
C	Updated with new PI style.	12/17

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