Application Note AN-302
Qspeed™ Family

Reverse Voltage Sharing of Series Diodes

Abstract

When reverse voltage is applied across two diodes connected in series, it divides across both devices–equally if they have similar electrical characteristics–once they are fully reverse biased. However, as they transition from the forward to the reverse biased state, the voltage across each device changes dynamically. This document describes the factors that affect dynamic voltage sharing of series connected diodes, and explains why co-packaged devices typically see little difference in the instantaneous voltages that develop across them, as they are quickly reverse-biased, under high-frequency, high $^{di}/_{dt}$ conditions typical in continuous conduction mode (CCM) boost converter operation.

Introduction

Reverse recovery charge (Q_{RR}) is a measure of the number of charge carriers that must be removed from a forward biased diode, as it begins to block the reverse voltage applied to it. Q_{RR} causes the diode's reverse recovery current (I_{RR}) and determines how much time (t_{RR}) reverse recovery takes. Since Q_{RR} directly determines t_{RR}, it is essential that the Q_{RR} and the t_{RR} of the two series diodes be the same, so that they both recover and begin to start blocking the applied reverse voltage (dynamically) at the same time, and at the same rate.

A Silicon diode's Q_{RR} is mainly caused by the minority carriers that are injected from the anode into the drift region and cathode of the device, as it conducts forward current. Those minority carriers eventually recombine with majority carriers in the drift region and cathode. The higher the forward current, the farther those minority carriers will travel and the longer they will persist, before they all recombine. When the diode is quickly turned off (particularly if the reverse voltage is high in magnitude), the suddenly applied reverse bias sweeps the minority carriers that have not yet recombined back across the junction and into the anode of the device. That produces the brief yet substantial I_{RR} that occurs until those minority carriers are gone and the diode starts blocking the reverse voltage.

The Q_{RR} of Silicon diodes varies with junction temperature, the magnitude of the applied reverse voltage, the amount of forward current being conducted when the device is reverse biased, and the rate at which the inductor current is commutated out of the diode (how quickly the reverse bias is applied). However, device junction temperature is the single factor that affects the Q_{RR} and t_{RR} of a Silicon diode more than any other.

Therefore, whenever identical Silicon diodes are connected in series, it is important to keep their junction temperatures as consistently equal as possible. Doing so ensures that the Q_{RR} and t_{RR} of both devices track each other closely, and that the dynamic voltage developed across each device will also track closely.

The Q_{RR} of Silicon diodes also varies with their semiconductor geometry and processing. The more reverse voltage the device must block, the thicker its drift region must be. For example, the drift region of a 600 V diode is about twice the thickness of a 300 V device. The thicker a diode's drift region is, the more minority carriers it will have in it when it is conducting high forward currents. That will give it a higher Q_{RR} than a diode that has a thinner drift region.

Series Connected Diodes

To reduce the Q_{RR} of a 600 V Silicon diode, two 300 V devices are often connected in series. This results in a Q_{RR} that is about the same as that of a single 300 V device. However, any applied reverse voltage is shared by both devices.

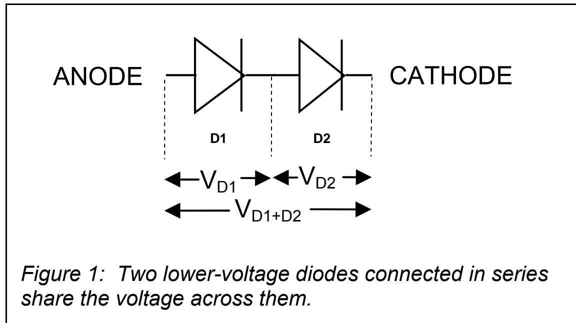

Figure 1: Two lower-voltage diodes connected in series share the voltage across them.

Factors that Affect Dynamic Reverse Voltage Sharing

Apart from the internal structure and processing of the semiconductor material and the boost circuit's operating parameters, the junction temperature of the die is the most influential factor on the Q_{RR} and the t_{RR} of the devices. The Q_{RR} of Silicon diodes have a positive temperature coefficient, which means that it will increase as the junction temperature of the die goes up. To ensure that two series diodes share the voltage across them equally, it is important to make their junction temperatures track each other very closely.

Besides making sure that the electrical characteristics of the die are as identical as possible (through good fabrication process design and control) careful attention to the design and assembly of the packaging can ensure that the die temperatures deviate much less than 2 °C from each other. Figure 2 is a plot of a simulation of the effects of temperature difference on the reverse voltage (V_R) of two series connected diode die, versus the junction temperature of both die, and the effects of a difference in the temperature (ΔT) between them.

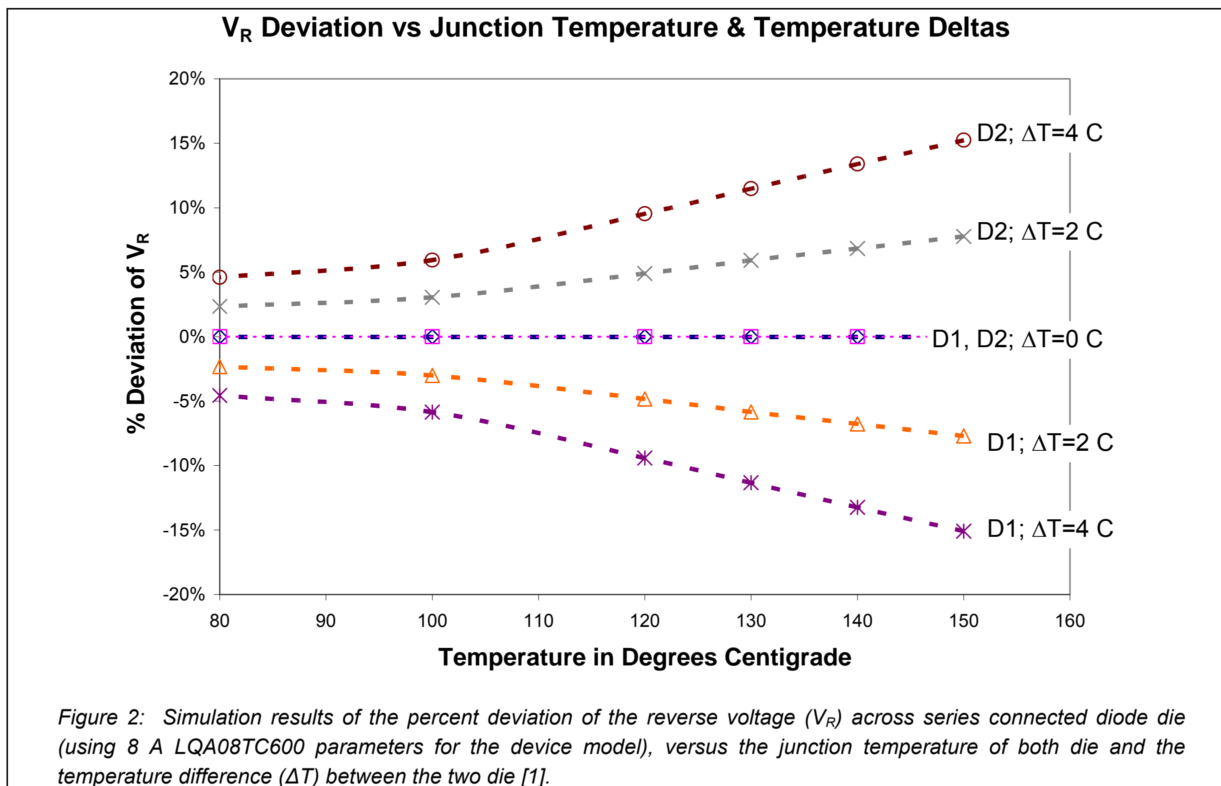

Figure 2: Simulation results of the percent deviation of the reverse voltage (V_R) across series connected diode die (using 8 A LQA08TC600 parameters for the device model), versus the junction temperature of both die and the temperature difference (ΔT) between the two die [1].

Row one of Table I contains the resulting dynamic voltages that would be impressed across each die in the worst-case condition of die junction temperatures being at their specified datasheet maximum (150 °C) with a deviation between the die temperatures that is more than twice what the package design maintains, to show the margin that has been built into the design of the packaging.

$D1_{T_JUNCTION}$ °C	$D2_{T_JUNCTION}$ °C	% Deviation V_R	$D1_{VR}$	$D2_{VR}$
154	150	+15	170 V	230 V
129	125	+10	180 V	220 V
114	110	+7.5	185 V	215 V

Table 1.

Even in such an extreme case, the deviation of the reverse voltage (V_R) across the cooler die (D2) will not be more than +15%, which would result in a maximum dynamic V_R of 230 V across the cooler of the two die. There is sufficient margin between 230 V and the 300 V maximum repetitive reverse voltage (V_{RRM}) rating of the die, which ensures that the avalanche voltage rating of the parts will not be exceeded.

In addition, most power supply design rules limit printed circuit board (PCB) temperatures to 100 °C. With adequate heatsinking, that would mean that the typical junction temperature of both die would not be likely to exceed 110 °C. At a junction temperature of 110 °C, there would be even more margin to the avalanche voltage rating of the die, since the V_R deviation would only be about 7.5% (Table I, third row). Even if the device junction temperatures were allowed to operate as high as 125 °C, there would still be plenty of margin to prevent the avalanche voltage rating of either die from being exceeded in the dynamic voltage sharing that occurs during the transition from the forward to the reverse biased condition (Table I, second row).

Finally, a thermal impedance (Z_θ) test is performed on all parts, after they are packaged, to ensure that a quality die attach has been made between each die and the substrate it is mounted to. This step ensures that the temperature difference between die will be minimal (typically « 2 °C).

Summary

As power diodes transition from the forward to the reverse biased state, the voltage across series connected devices changes dynamically. However, when die with very consistent electrical characteristics are mounted in close proximity to each other, their temperature difference and the variation of their individual Q_{RR}, and t_{RR} are minimized, and the reverse voltage that dynamically that appears across them, as they become reverse biased, develops very equally. Therefore, it is extremely unlikely that enough voltage will develop across either diode quickly enough to exceed its avalanche voltage rating before the other has recovered enough to prevent such an occurrence. In real-world operation, no such failures have occurred in any Q-Series devices.

References

1. The device V_R deviation was simulated using Dios and Dessis (TCAD tools from Synopsys, Inc), for process and device simulation, respectively. The Traps model, implemented in Dessis, was used to account for the recombination centers that are designed into the die structure. The model parameters used in simulation were derived from the work by Lutz and et al ("Irradiation-Induced Deep Levels in Silicon for Power Device Tailoring," *Journal of The Electrochemical Society, 153 (2) G108-G118, 2006*).

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Revision	Notes	Date
1.2	Released by Qspeed	01/08
1.3	Converted to Power Integrations Document	01/11

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